MELSEC-L Series

Programmable Logic Controllers

User's Manual

IO-Link Master Module
ME1IOL6-L

Art. no.: 254015
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Version A

Version check

About this Manual

The texts, illustration, diagrams and examples in this manual are provided for information purposes only. They are intended as aids to help explain the installation, operation, programming and use of the programmable logic controllers of the MELSEC-L series.

If you have any questions about the installation and operation of any of the products described in this manual please contact your local sales office or distributor (see back cover).
You can find the latest information and answers to frequently asked questions on our website at www.mitsubishi-automation.com.

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User's Manual
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Version			Changes / Additions / Corrections
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Safety Guidelines

For use by qualified staff only

This manual is only intended for use by properly trained and qualified electrical technicians who are fully acquainted with the relevant automation technology safety standards. All work with the hardware described, including system design, installation, configuration, maintenance, service and testing of the equipment, may only be performed by trained electrical technicians with approved qualifications who are fully acquainted with all the applicable automation technology safety standards and regulations. Any operations or modifications to the hardware and/or software of our products not specifically described in this manual may only be performed by authorised Mitsubishi Electric staff.

Proper use of the products

The programmable logic controllers of the MELSEC-L series are only intended for the specific applications explicitly described in this manual. All parameters and settings specified in this manual must be observed. The products described have all been designed, manufactured, tested and documented in strict compliance with the relevant safety standards. Unqualified modification of the hardware or software or failure to observe the warnings on the products and in this manual may result in serious personal injury and/or damage to property. Only peripherals and expansion equipment specifically recommended and approved by Mitsubishi Electric may be used with the programmable logic controllers of the MELSEC-L series.

All and any other uses or application of the products shall be deemed to be improper.

Relevant safety regulations

All safety and accident prevention regulations relevant to your specific application must be observed in the system design, installation, configuration, maintenance, servicing and testing of these products. The installation should be carried out in accordance to applicable local and national standards.

Safety warnings in this manual

In this manual warnings that are relevant for safety are identified as follows:

DANGER:

Failure to observe the safety warnings identified with this symbol can result in health and injury hazards for the user.

WARNING:

Failure to observe the safety warnings identified with this symbol can result in damage to the equipment or other property.

General safety information and precautions

The following safety precautions are intended as a general guideline for using PLC systems together with other equipment. These precautions must always be observed in the design, installation and operation of all control systems.

DANGER:

- ***Observe all safety and accident prevention regulations applicable to your specific application. Always disconnect all power supplies before performing installation and wiring work or opening any of the assemblies, components and devices.***
- ***Assemblies, components and devices must always be installed in a shockproof housing fitted with a proper cover and fuses or circuit breakers.***
- ***Devices with a permanent connection to the mains power supply must be integrated in the building installations with an all-pole disconnection switch and a suitable fuse.***
- ***Check power cables and lines connected to the equipment regularly for breaks and insulation damage. If cable damage is found immediately disconnect the equipment and the cables from the power supply and replace the defective cabling.***
- ***Before using the equipment for the first time check that the power supply rating matches that of the local mains power.***
- ***Take appropriate steps to ensure that cable damage or core breaks in the signal lines cannot cause undefined states in the equipment.***
- ***You are responsible for taking the necessary precautions to ensure that programs interrupted by brownouts and power failures can be restarted properly and safely. In particular, you must ensure that dangerous conditions cannot occur under any circumstances, even for brief periods.***
- ***EMERGENCY OFF facilities conforming to EN 60204/IEC 204 and VDE 0113 must remain fully operative at all times and in all PLC operating modes. The EMERGENCY OFF facility reset function must be designed so that it cannot ever cause an uncontrolled or undefined restart.***
- ***You must implement both hardware and software safety precautions to prevent the possibility of undefined control system states caused by signal line cable or core breaks.***
- ***When using modules always ensure that all electrical and mechanical specifications and requirements are observed exactly.***

Contents

1 Overview

This User's Manual describes the specifications, handling and programming methods for the IO-Link Master Module ME1IOL6-L (hereinafter referred to as the ME1IOL6-L) which is used with the programmable controllers of the MELSEC-L series.

Before using the ME1IOL6-L, please read this manual and the relevant manuals carefully and develop familiarity with the functions and performance of the MELSEC-L series programmable controller to handle the product correctly.

1.1 IO-Link System Overview

The ME1IOL6-L is a master module for IO-Link. Up to six IO-Link devices (slaves) or conventional I/O devices can be connected to a single ME1IOL6-L.

An IO-Link system consists of IO-Link devices (often sensors, actuators or combinations thereof), a standard 3-wire sensor/actuator cable and an IO-Link master.

Only one IO-Link device can be connected to each port of the master. Thus IO-Link is point-to-point communication and not a fieldbus.

1.1.1 Data exchange in an IO-Link System

Two types of data may basically be exchanged:

- Cyclic data (process data)
- Acyclic data (service data)

Cyclic data is exchanged automatically. Acyclic data is exchanged only after a request of the IO-Link master.

Process data

Process data can be comprised of process input data and/or process output data. The process data of the devices is transmitted cyclically in a data frame. In some cases the process data is split up and transmitted in several cycles.

A diagnostic flag indicates that the process data is invalid.

Service data

Service data can be comprised of on-request data objects and events. Service data is always exchanged acyclically and always upon request of the IO-Link master. First, the IO-Link master sends a request to the device and the device responds. This is true for writing data to the device as well as for reading data from the device. Service data can be used to read out parameter values or device states. It can also be used to write parameter values or to send commands.

When an event occurs the device notifies the master. The master responds and reads out the reported event. This means that events or device states such as low supply voltage, short circuit, etc. can be transmitted via the IO-Link master to the PLC.

More information

This short overview about IO-Link is only a extract of the information provided on the website of the IO-Link Consortium. You can find much more information about IO-Link and answers to frequently asked questions on their website at www.io-link-com.

1.2 Features of the ME1IOL6-L

IO-Link master function

Up to six IO-Link devices can be connected to a single ME1IOL6-L.

Various modes selectable

Each channel of the ME1IOL6-L can be configured to run in IO-Link mode, in digital input mode (SIO mode), digital output mode (SIO mode) or can be deactivated.

Useful functions for data input and output

The following functions are available in IO-Link mode:

- Automatic update of input and output process data
- Exchange of consistent data
- Masking of input data
- Data valid output HOLD/CLEAR
- Data swapping

In SIO mode, the HOLD/CLEAR function is available in output mode.

Acyclic communication

In addition to the cyclic communication between the IO-Link master and an IO-Link device, data can be exchanged using acyclic communication.

Convenient functions associated with IO-Link devices

- Direct parameter page access
- Automatic confirmation of events
- Data storage for automatic IO-Link devices parameter back-up
- Device validation

For a detailed description of the functions of the ME1IOL6-L, please refer to section 4.3.

2 System Configuration

2.1 Overall System Configuration

The following shows a system configuration example for using the IO-Link master module.

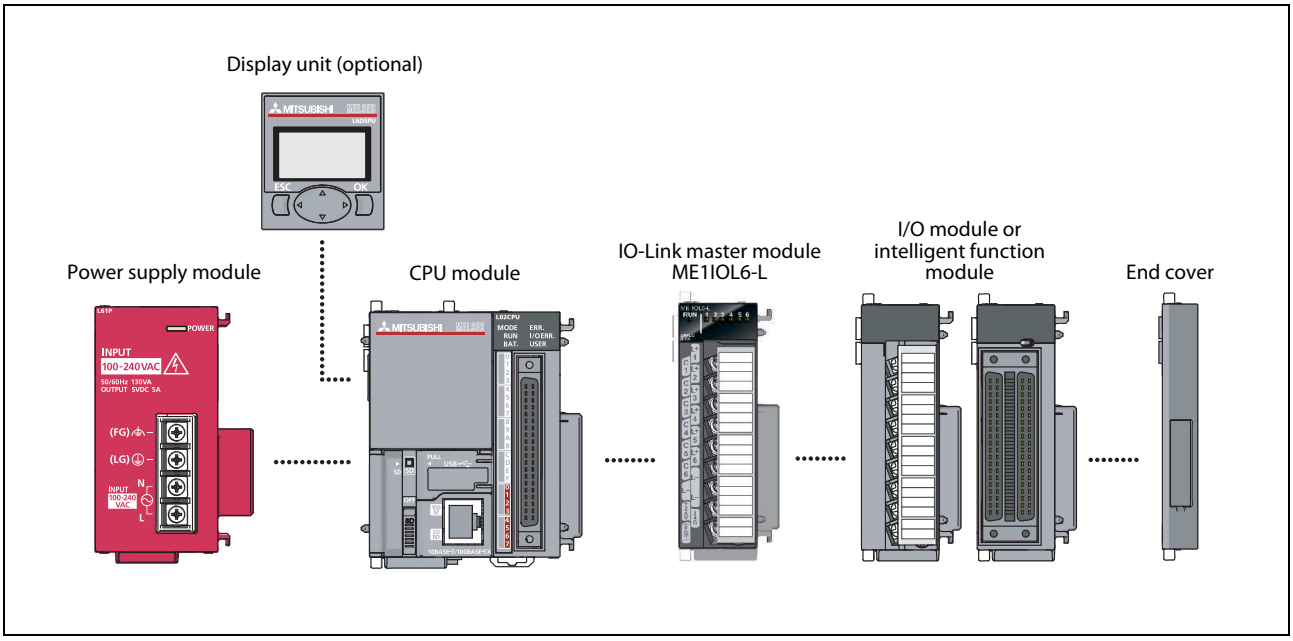


Fig. 2-1: *Connection of the ME1IOL6-L to a CPU module*

For the installation of the PLC and the mounting of modules, please refer to the User's Manual for the CPU modules of the MELSEC-L series (Hardware design, Maintenance and Inspection).

2.2 Applicable System

Number of connectable modules

The number of I/O modules and intelligent function modules that can be connected in a system is 10 in total*. If more than 10 modules are connected, the CPU module detects "SP.UNIT LAY ERR." (error code: 2124).

* The number of modules is exclusive of the number of power supply modules, CPU modules, display units, RS-232 adapters, and END covers.

There is no restriction on the number of IO-Link master modules ME1IOL6-L as long as the total number of modules is 10 or less.

Compatible software version

For the programming and monitoring of ME1IOL6-L installed in a MELSEC-L series PLC use GX Works2. GX Developer can also be used.

3 Quick start IO-Link

This chapter explains based on a simple programming example how to start IO-Link communication with the IO-Link Master.

A comprehensive description can be found in chapter 5 of this manual.

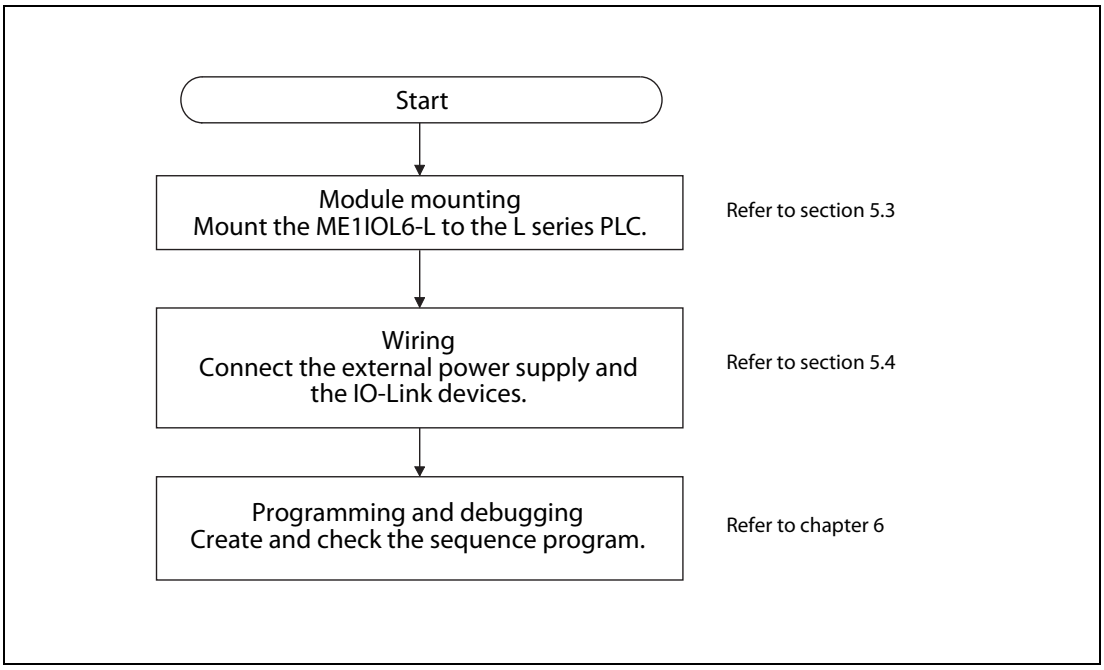


Fig. 3-1: *Function chart for the setup of an IO-Link master module ME1IOL6-L*

3.1 Enabling IO-Link communication

After setting the IO-Link master to IO-Link mode, IO-Link communication with the connected IO-Link Devices is started. Please note that in the following example the ME1IOL6-L occupies the input and output addresses X/Y40 to X/Y5F.

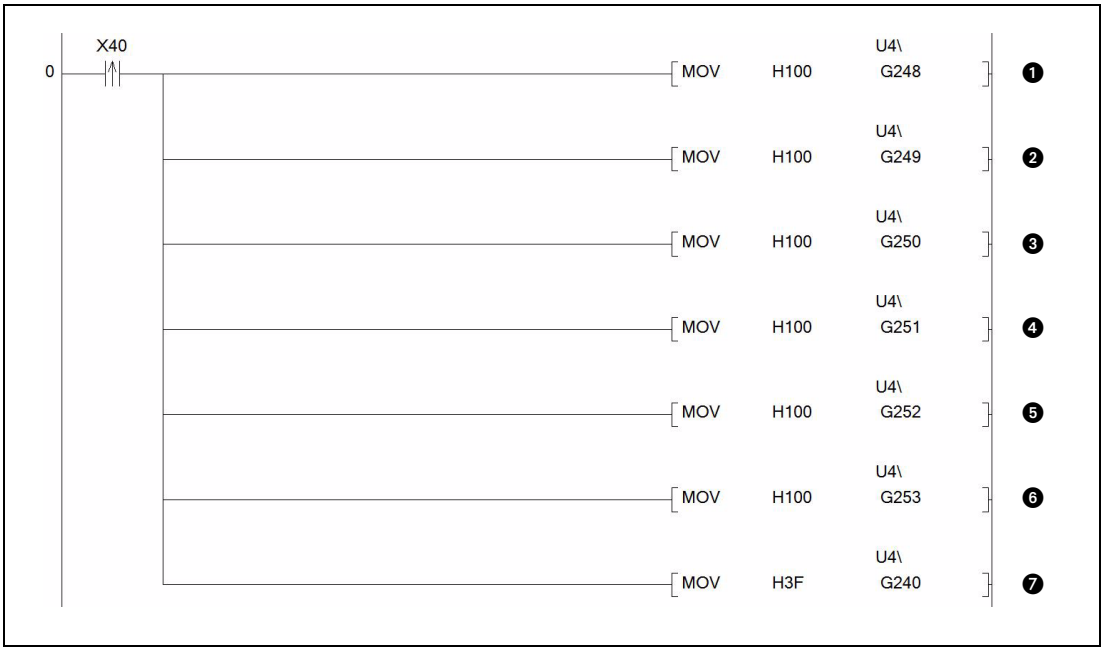


Fig. 3-2: *Settings for channels CH1 to CH6*

Number	Description	
❶	The relevant channel set to: IO-Link mode, data swapping, fastest possible cycle time	Channel CH1
❷		Channel CH2
❸		Channel CH3
❹		Channel CH4
❺		Channel CH5
❻		Channel CH6
❼	The channel mode change flags for CH1 to CH6 are set.	

Tab. 3-1: *Description of the program for the settings*

3.2 Verifying IO-Link communication

The current mode of each channel can be checked in the current mode registers:

Address		Description		Value													
Hexa-decimal	Decimal			High Byte								Low Byte					
110H	272	CH1	Current mode	0	0	0	0	0	0	0	1	0	0	0	1	0	1	1	1
111H	273	CH2		0	0	0	0	0	0	0	1	0	0	0	1	0	1	1	1
112H	274	CH3		0	0	0	0	0	0	0	1	0	0	0	1	0	1	1	1
113H	275	CH4		0	0	0	0	0	0	0	1	0	0	0	1	0	1	1	1
114H	276	CH5		0	0	0	0	0	0	0	1	0	0	0	1	0	1	1	1
115H	277	CH6		0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	1
											↑								
											Bit 8: 1 = IO-Link mode								

Tab. 4-2: *Value of the current mode registers*

Please note, that the low byte values in the above table are depending on the cycle time settings of your current configuration and can differ from the shown status of the bits.

Active IO-Link communication with a connected device is shown in the channel diagnostic registers:

Address		Description		Value															
Hexa-decimal	Decimal			High Byte								Low Byte							
11BH	283	CH1	Diagnostic information	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
11CH	284	CH2		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
11DH	285	CH3		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
11EH	286	CH4		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
11FH	287	CH5		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
120H	288	CH6		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
												↑							
												Bit 7: 1 = Device connected							

Tab. 4-3: *Value of the channel diagnostic registers*

NOTE Refer to section 4.5.1 for buffer memory assignment.

3.3 Input process data

The input process data is received from the IO-Link Device and written to the buffer memory automatically.

Address		Description		High byte	Low byte
Hexa-decimal	Decimal				
0H	0	CH1	Input process data in IO-Link mode	Byte 1	Byte 0
1H	1			Byte 3	Byte 2
to	to			⋮	⋮
FH	15			Byte 31	Byte 30
10H	16	CH2	Input process data in IO-Link mode	Byte 1	Byte 0
to	to			⋮	⋮
1FH	31			Byte 31	Byte 30
20H	32	CH3	Input process data in IO-Link mode	Byte 1	Byte 0
to	to			⋮	⋮
2FH	47			Byte 31	Byte 30
30H	48	CH4	Input process data in IO-Link mode	Byte 1	Byte 0
to	to			⋮	⋮
3FH	63			Byte 31	Byte 30
40H	64	CH5	Input process data in IO-Link mode	Byte 1	Byte 0
to	to			⋮	⋮
4FH	79			Byte 31	Byte 30
50H	80	CH6	Input process data in IO-Link mode	Byte 1	Byte 0
to	to			⋮	⋮
5FH	95			Byte 31	Byte 30

Tab. 3-4: *Input process data allocation in buffer memory (data swap enabled)*

If the input data invalid flags in IO-Link mode are showing a high signal either there is no IO-Link communication or the input process data is marked as invalid by the IO-Link Device.

Signal direction CPU Module ← ME1IOL6-L																
Device No. (Input)	Value															
	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
X40–X4F	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1
X50–X5F	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

X51: CH1 input data is valid
X52: CH2 input data is valid
X53: CH3 input data is valid
X54: CH4 input data is valid
X55: CH5 input data is valid
X56: CH6 input data is valid

Tab. 4-5: *Value of the input devices*

3.4 Output process data

The output process data stored in the buffer memory is sent to the IO-Link Device automatically.

Address		Description		High byte	Low byte
Hexa-decimal	Decimal				
70H	112	CH1	Output process data in IO-Link mode	Byte 1	Byte 0
71H	113			Byte 3	Byte 2
to	to			⋮	⋮
7FH	127			Byte 31	Byte 30
80H	128	CH2	Output process data in IO-Link mode	Byte 1	Byte 0
to	to			⋮	⋮
8FH	143			Byte 31	Byte 30
90H	144	CH3	Output process data in IO-Link mode	Byte 1	Byte 0
to	to			⋮	⋮
9FH	159			Byte 31	Byte 30
A0H	160	CH4	Output process data in IO-Link mode	Byte 1	Byte 0
to	to			⋮	⋮
AFH	175			Byte 31	Byte 30
B0H	176	CH5	Output process data in IO-Link mode	Byte 1	Byte 0
to	to			⋮	⋮
BFH	191			Byte 31	Byte 30
C0H	192	CH6	Output process data in IO-Link mode	Byte 1	Byte 0
to	to			⋮	⋮
CFH	207			Byte 31	Byte 30

Tab. 3-6: *Output process data allocation in buffer memory (data swap enabled)*

In case of IO-Link process output data the IO-Link master needs to send an output data valid to the IO-Link device. For this purpose it is necessary to set the appropriate signals:

Signal direction CPU Module → ME1IOL6-L																
Device No. (Output)	Value															
	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Y40–Y4F	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Y50–Y5F	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0

Y51: CH1 output data is valid
Y52: CH2 output data is valid
Y53: CH3 output data is valid
Y54: CH4 output data is valid
Y55: CH5 output data is valid
Y56: CH6 output data is valid

Tab. 4-7: *Value of the output devices*

NOTE Refer to section 4.5.1 for buffer memory assignment and section 4.4.1 for the list of I/O signals.

4 Detailed Description of the Module

4.1 Part Names

This section explains the names of the components for the ME1IOL6-L

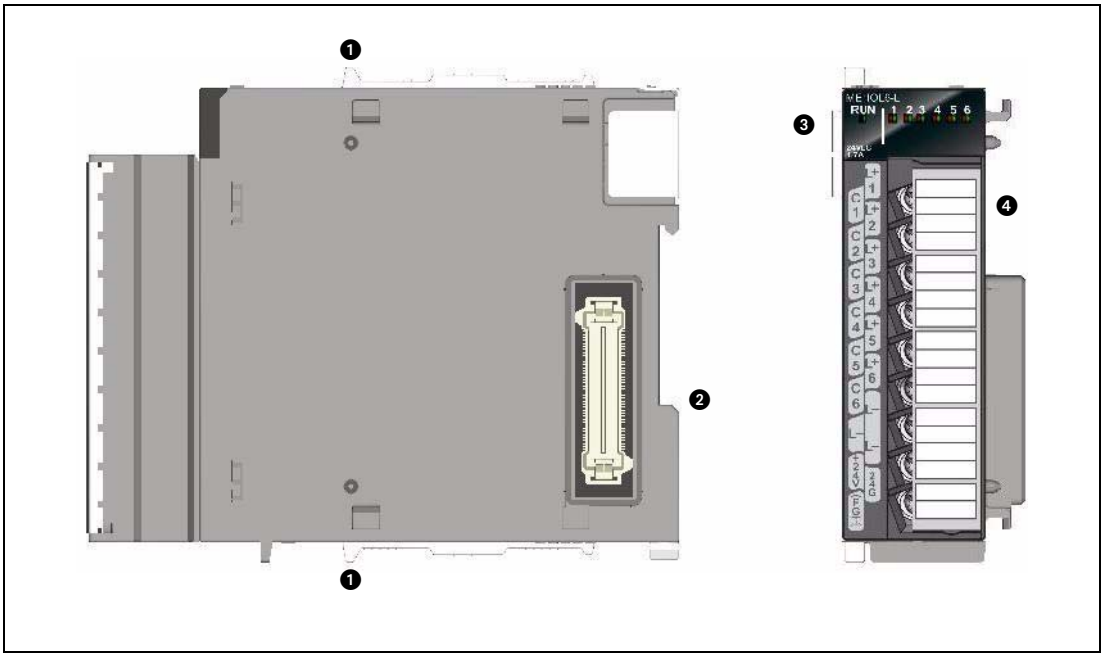


Fig. 4-1: *Names of parts*

No.	Name		Description		
❶	Module joint levers		Levers for connecting two modules		
❷	DIN rail hook		A hook used to mount the module to a DIN rail.		
❸	LEDs	RUN	Displays the operating status of the ME1IOL6-L. On: Normal operation Off: – Internal power supply (5 V DC) is OFF. – External power supply (24 V DC) is OFF. – An internal error has occurred.		
		1 to 6	Indicates the I/O status of each channel of the ME1IOL6-L.		
			SIO mode	On (red):	An error has occurred on this channel.
				On (green):	Input/output signal is ON
				Off:	Input/output signal is OFF
			IO-Link mode	On (red):	An error has occurred on this channel.
				Flashing (green):	Channel does IO-Link communication
				Off:	– Not connected
❹	Detachable terminal block		Used for connection of the sensors or actuator and the external power supply.		
	Terminal cover		A cover for preventing touching the terminals. A label on it is used for recording the signal names of devices allocated to terminals.		

Tab. 4-1: *Description of the parts of the ME1IOL6-L*

4.1.1 Signal Layout of the Terminal Block

Terminal No.	Signal name		Description	
1	CH1	L+1	+24 V DC	Power supply output for connected sensor/actuator
2		C1	SIO mode	Switching signal DI/DO
			IO-Link mode	"Coded switching" (Communication line)
3	CH2	L+2	+24 V DC	Power supply output for connected sensor/actuator
4		C2	SIO mode	Switching signal DI/DO
			IO-Link mode	"Coded switching" (Communication line)
5	CH3	L+3	+24 V DC	Power supply output for connected sensor/actuator
6		C3	SIO mode	Switching signal DI/DO
			IO-Link mode	"Coded switching" (Communication line)
7	CH4	L+4	+24 V DC	Power supply output for connected sensor/actuator
8		C4	SIO mode	Switching signal DI/DO
			IO-Link mode	"Coded switching" (Communication line)
9	CH5	L+5	+24 V DC	Power supply output for connected sensor/actuator
10		C5	SIO mode	Switching signal DI/DO
			IO-Link mode	"Coded switching" (Communication line)
11	CH6	L+6	+24 V DC	Power supply output for connected sensor/actuator
12		C6	SIO mode	Switching signal DI/DO
			IO-Link mode	"Coded switching" (Communication line)
13	L-		0 V	Power supply output for connected sensors/actuators
14	L-			
15	L-			
16	+ 24V		+24 V DC	External power supply input
17	24G		0 V	
18	(FG)		Frame Ground	

Tab. 4-2: *Signal layout for the detachable terminal block of the ME1IOL6-L*

For the wiring of the IO-Link master module ME1IOL6-L please refer to section 5.4.

4.2 Specifications

The specifications for the ME1IOL6-L are shown in the following table. For general specifications, please refer to the User's Manual for the CPU modules of the MELSEC-L series (Hardware design, Maintenance and Inspection).

Item			Specifications	
Number of ports			6	
Port configuration			• IO-Link • Digital output (SIO mode) • Digital input (SIO mode) • Disabled	
IO-Link mode		Rated voltage	24 V DC	
		Rated output current (C/Q)	15 mA	
		Rated sensor/actuator supply current (L+)	200 mA	
SIO mode	Digital input	Input type	Sink	
		Rated voltage	24 V DC	
		Internal pull-down current (C/Q)	5 mA	
		Input filter (HW and SW)	200 µs	
	Digital output	Rated voltage	24 V DC	
		Rated output current (C/Q)	200 mA	Max. current per port (sum of C and L+): 215 mA
		Rated sensor/actuator supply current (L+)	200 mA	
		Output type	Push-pull	
Port disabled		Communication line (C/Q)	Switched OFF	
		Sensor/actuator supply line (L+)		
Protection functions	Communication line (C/Q)		Over-current, over-load and short-circuit	
	Sensor/actuator supply line (L+)			
Insulation method	Between the I/O terminals and PLC power supply		Photocoupler isolation	
	Between channels		No isolation	
Dielectric withstand voltage			Between I/O terminals and programmable controller power supply: 500 V AC_{rms} for 1 minute	
Insulation resistance			Between I/O terminals and programmable controller power supply: 500 V DC, 10 MΩ or more	
Number of occupied I/O points			32 points (I/O assignment: Intelligent 32 points)	
External wiring connection system			18-points terminal block	
Cable specification		Cable type	Unshielded cable	
		Maximum length	20 m	
		Applicable wire size	0.3 to 0.75mm^2	
		Overall loop resistance	6 Ω	
		Effective line capacitance	3 nF	
Applicable solderless terminals			R1.25-3 (Solderless terminals with sleeves cannot be used.)	
External supply power		Voltage	24 V DC (+20%, -15%); ripple, spike within 500mV_{P-P} In order to keep the specified IO-Link output voltage levels (L+ line) the external supply voltage must be higher than 22 V DC.	
		Current	The sum current on the L- lines must not exceed 1.7 A.	
		Inrush current	8 A within 230 µs	
Internal current consumption (5 V DC)			0.4 A	
Online module change			Not supported	
Weight			180 g	

Tab. 4-3: *Specifications of the ME1IOL6-L*

4.2.1 External Dimensions

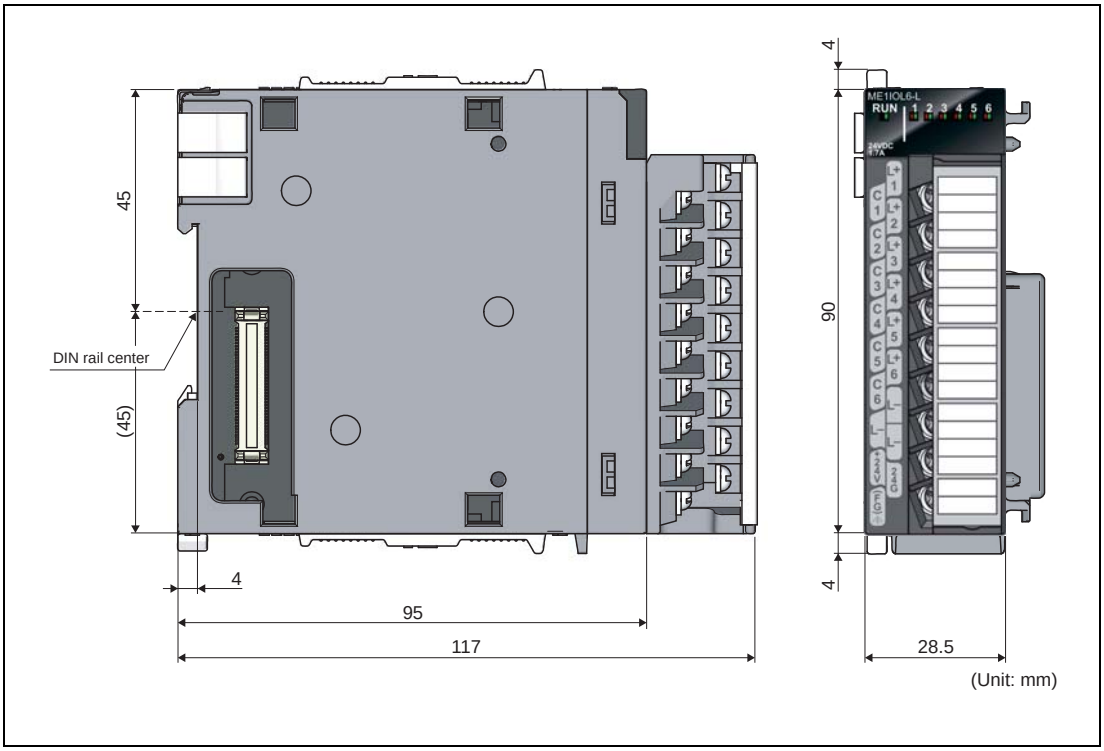


Fig. 4-2: *Dimensions of the ME1IOL6-L*

4.3 Functions of the IO-Link Master Module

Function	Description	Reference
IO-Link master function	• Communication with IO-Link devices Up to six IO-Link devices can be connected to a single ME1IOL6-L. • FDT/DTM function support Using a commercially available FDT (Field Device Tool), reading/writing the IO-Link device's parameters and monitoring the IO-Link device status are executable via the ME1IOL6-L.	Section 4.3.1
Various modes selectable	Each channel of the ME1IOL6-L can configured to run in IO-Link mode, in Standard I/0 mode (SIO mode) or can be deactivated.	Section 4.3.2
Masking of input data	To recognize certain bits in the first two bytes of the input data, an input data mask can be used to filter the input process data. The result is shown for each channel on an input signal.	Section 4.3.3
Output HOLD/CLEAR	The output status can be retained when the PLC CPU module is placed in the STOP status or when an error occurs.	Section 4.3.4
Data swapping	For communication with an IO-device, the order of bytes can be changed for each channel.	Section 4.3.5
Exchange of consistent data	The exchange of more than two bytes of process data in a consistent way or the synchronization between reading input data and writing output data is possible by using the consistency handshake signals provided by the ME1IOL6-L.	Section 4.3.6
Acyclic communication	In addition to the cyclic communication between the IO-Link master and an IO-Link device, data can be exchanged using acyclic communication.	Section 4.3.7
Direct parameter page access	The direct parameter page 1 of an IO-Link device can be accessed by using the acyclic communication interface or the direct mapping in the buffer memory.	Section 4.3.8
Automatic confirmation of events	By sending event data to the IO-Link master, an IO-Link device can inform about warnings, errors or certain states. The ME1IOL6-L can confirm these events automatically.	Section 4.3.9
Data storage	The ME1IOL6-L can backup parameter data from the IO-Link device and also can write these data back to the device.	Section 4.3.10
Device validation	When the device validation is activated the ME1IOL6-L checks the connected IO-Link device at every start-up of the IO-Link communication. A device error is indicated by the ME1IOL6-L in case that the validation is not successful.	Section 4.3.11

Tab. 4-4: *Functions of the ME1IOL6-L*

4.3.1 IO-Link Master Function

Up to six IO-Link devices or conventional devices can be connected to a single ME1IOL6-L.

In IO-Link mode process data (e.g. analog values, switching states) are exchanged cyclically, configuration data (e.g. activation, deactivation of functions) as well as identification data (manufacturer ID) typically at startup, and parameters or diagnostics are sent as needed (acyclic communication).

FDT/DTM function support

Using a commercially available FDT, reading/writing the IO-Link device parameters and monitoring the IO-Link device status are executable via the ME1IOL6-L.

Refer to section 5.6 (Setting of the IO-Link devices) for more details about the FDT/DTM* system structure.

* FDT stands for **F**ield **D**evice **T**ool and DTM stands for **D**evice **T**ype **M**anager. FDT/DTM is a communication technique for the manufacturer-independent configuration of field devices.

4.3.2 Input and Output Data in IO-Link Mode or SIO Mode

Each channel of the ME1IOL6-L can configured to run either in IO-Link mode or in Standard I/0 mode (SIO mode) as digital input or digital output. Mixed operation of IO-Link and conventional devices is

possible. A channel can also be deactivated. In this case, the 24 V DC voltage output on the channels L+ line is switched OFF.

To change the mode of a channel of the IO-Link master module, the user has to set the corresponding mode change bit of the channel in the buffer memory address Un\G240. The module will try to change the mode and stores the result of the operation in an other buffer memory address. For more information about the mode changing please refer to section 4.5.6.

IO-Link mode

- Input data

  In IO-Link mode, the input process data (up to 32 bytes per channel) from the connected IO-Link device is stored in the buffer memory of the ME1IOL6-L. The size and the structure of the data depends on the connected device. Therefore, the ME1IOL6-L maps the data straight into the input process data area without any interpretation (refer to section 4.5.2).

  In case that IO-Link communication stops (e.g. due to undervoltage, disconnection of an IO-Link Device) the input process data buffer is set to 0.

- Output data

  In IO-Link mode, output process data (up to 32 bytes per channel) stored in the buffer memory is output to the connected IO-Link device. The size and the structure of the data depends on the connected device.

  To send output data to the IO-Link device it is necessary to set the corresponding data valid signal Y(n+1)1 to Y(n+1)6 (refer to section 4.4). The behaviour of these output signals in case of a PLC stop when the output data in the buffer memory is no longer refreshed can be defined by the intelligent function module switch no. 3 (refer to section 5.5.2).

SIO mode

- SIO input mode

  In SIO input mode the state of the digital input signal of each channel is shown on the input signals Xn1 to Xn6 (refer to section 4.4).

- SIO output mode

  When a channel is running in SIO output mode, the output signal can be driven by the according output signal Yn1 to Yn6. The status of the signal is reflected by the channel's LED.

  The behaviour of these output signals in case of a PLC stop (output OFF or hold) can be defined by the intelligent function module switch no. 3 (refer to section 5.5.2).

4.3.3 Masking of Input Data

To recognize certain bits in the first two bytes of the input data, an input data mask can be used to filter the input process data. For each channel one mask composed of two bytes is provided (section 4.5.4).

The IO-Link master module will perform the following operation between the mask and the first two bytes of input process data for the corresponding channel (refer to section 4.5.2):

[(Input data) AND (Input mask)] XOR (Input mask) = $\overline{Xn}$

The result of this operation will be shown for each channel by the signals Xn1 to Xn6 (section 4.4).

The signal Xn will be "1" if at least each bit in process data input is set to "1" where the same bit in the input data mask is set to "1".

The following example will illustrate this logical operations. In this example, the input signal Xn is used to notify the PLC that the bit 3 of the input is set to "1".

- No match between the input data mask and the input data

Step	Description	Operation		Xn
		High byte	Low byte	
❶	Input data	0110 1111	1011 0001	
	Input data mask	0000 0000	0000 1000	
	AND operation	0000 0000	0000 0000	
❷	Result of the AND operation	0000 0000	0000 0000	
	Input data mask	0000 0000	0000 1000	
	XOR operation	0000 0000	0000 1000	**OFF**

Tab. 4-5: *Example for masking input data (no match)*

Number	Description
❶	A bitwise AND operation between the input data and the input data mask is performed.
❷	A bitwise XOR operation between the result of the AND operation and the input data mask is performed. Since a bit is set in the result of the XOR operation, the input signal Xn is switched OFF.

Tab. 4-6: *Explanation for the example*

- Match between the input data mask and the input data

Step	Description	Operation		Xn
		High byte	Low byte	
❶	Input data	0111 1001	0010 1010	
	Input data mask	0000 0000	0000 1000	
	AND operation	0000 0000	0000 1000	
❷	Result of the AND operation	0000 0000	0000 1000	
	Input data mask	0000 0000	0000 1000	
	XOR operation	0000 0000	0000 0000	**ON**

Tab. 4-7: *Example for masking input data (match)*

Number	Description
❶	A bitwise AND operation between the input data and the input data mask is performed.
❷	A bitwise XOR operation the result of the AND operation and the input data mask is performed. Since no bit is set in the result of the XOR operation, the input signal Xn is switched ON.

Tab. 4-8: *Explanation for the example*

An input data mask is only active if their value is greater than 0.

The byte order of the process data in buffer memory can be swapped (refer to section 4.3.5). This takes impact also on the input mask operation. When using the input mask on a channel which runs with reverse byte order (Data align flag = "1"), the input mask should be set in reverse byte order too.

The following figure shows the mask operation and the dependency to the byte order of the input data.

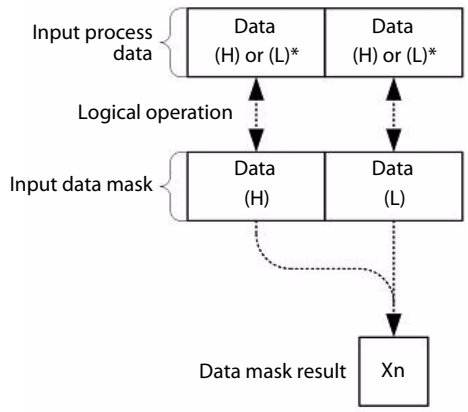


Fig. 4-3:
If the bits set to "1" in the input data mask are set also in the first two bytes of the input data, the data mask result is set to "1".

4.3.4 Output HOLD/CLEAR Function

For the case where the programmable controller (PLC) CPU is placed in STOP or in a stop error status, whether to hold (HOLD) or clear (CLEAR) the outputs can be set.

Make the setting in the HOLD/CLEAR setting of the intelligent function module switch (please refer to section 5.5.2).

Switch 3 is used to define the behaviour of the

– output signals Yn1 to Yn6 (SIO output mode) and the

– output data valid signals Y(n+1)1 to Y(n+6)1 (IO-Link mode)

4.3.5 Data Swapping Function

This is a function to exchange (swap) the upper and lower bytes of the process data and on-request-data (acyclic data) stored in the buffer memory of the ME1IOL6-L and the IO-Link device.

With this function, the word data processing need not swap the bytes using the sequence program for IO-Link devices storing the data in a reversed order.

The following figure shows the data flow and the swapping functionality of the ME1IOL6-L.

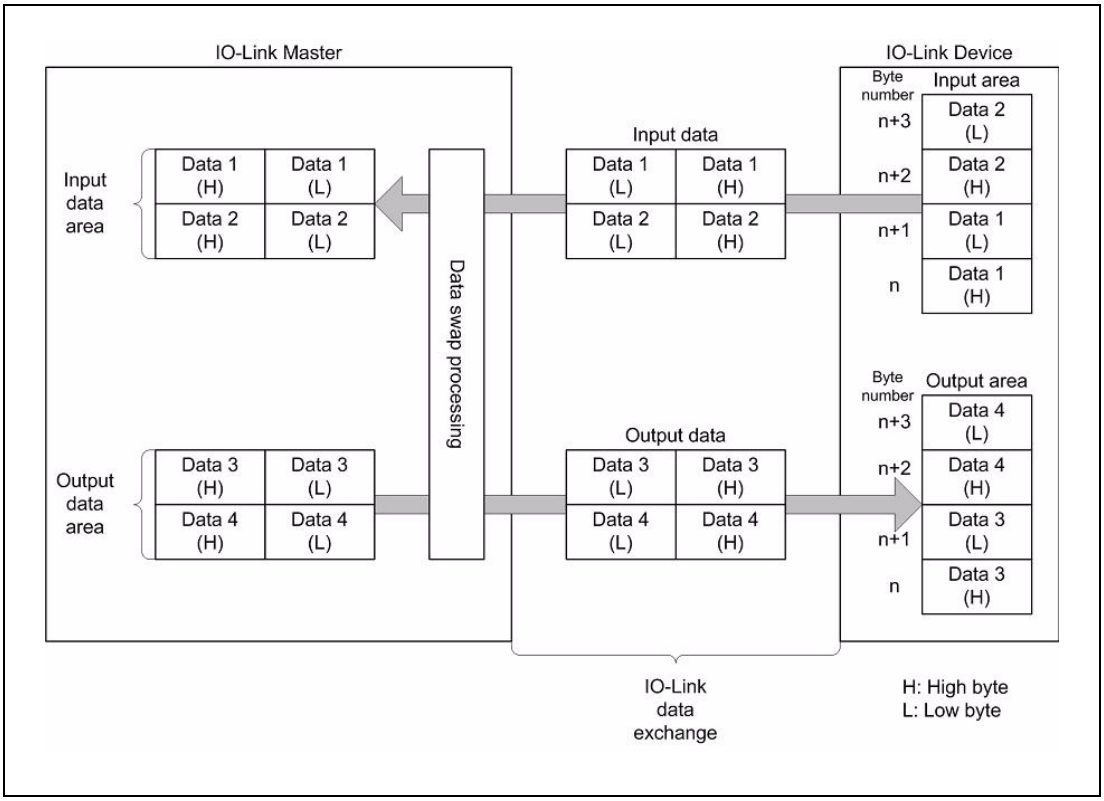


Fig. 4-4: *In this figure the data swapping is activated.*

Swapping of data can be enabled or disabled for each channel of the ME1IOL6-L. The function is controlled by the data align flag in the mode setting register (buffer memory addresses Un\G248 to Un\G253, refer to section 4.5.6).

By default (Data align = 0 = Data swapping active), the contents of the high and low byte is swapped. This operation is shown in the above figure.

If Data align is set to 1, the swapping is disabled and the byte order of the data bytes in buffer memory will be the same as coming from the device.

4.3.6 Exchange of Consistent Data

To exchange more than two bytes of process data in a consistent way or to have a synchronization between reading input data and writing output data it is necessary to use the consistency handshake signals provided by the ME1IOL6-L.

Using these signals ensures that the master will not update the process data during reading or writing from/to buffer memory.

The handshake signals can be used for input and output separately. The interaction of the signals is shown in the following figure.

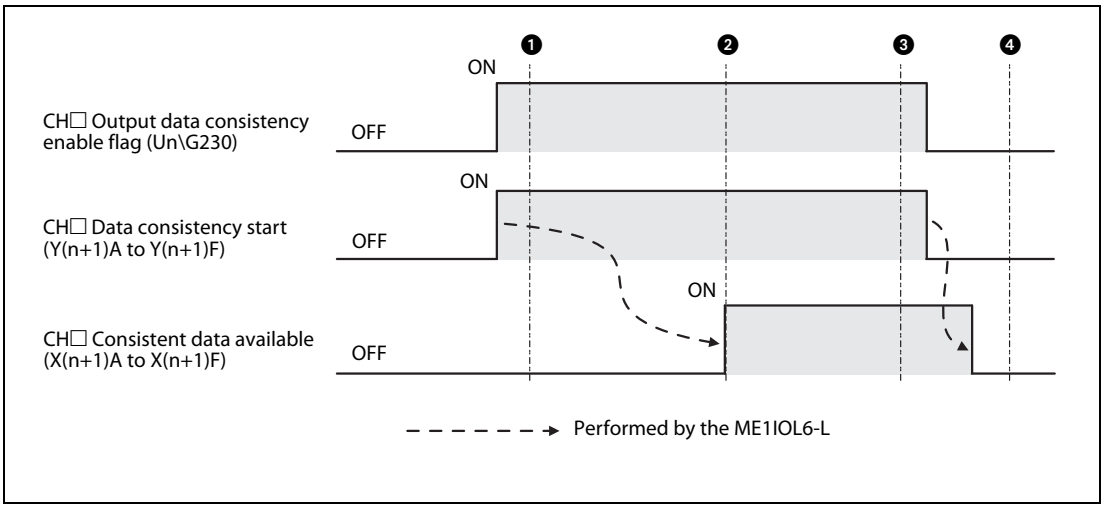


Fig. 4-5: *Timing of the data consistency signals*

Number	Description	
	Input data	**Output data**
❶	The PLC sets the CH☐ Output data consistency start flag and requests consistency for input data.	The CH☐ Output data consistency enable flag is always ON. For each step/cycle the setting of the CH☐ Output data consistency start flag is required for the consistency of the output data.
❷	The ME1IOL6-L stops updating the buffer memory.	The output of new data is stopped.
❸	PLC reads inputs.	PLC can set output data.
❹	ME1IOL6-L reads input data.	ME1IOL6-L sends output data.

Tab. 4-9: *Explanation for the example*

Each IO-Link channel of the ME1IOL6-L can be used independently.

For requesting consistent input process data only, it is sufficient to set the concerning data consistency start signal (Y(n+1)A to Y(n+1)F) and wait until the consistent data available signal (X(n+1)A to X(n+1)F) is turned ON.

To request the writing of consistent output data, the user has to set the output data consistency enable flag in the buffer memory address Un\G230 (section 4.5.5). The output data from buffer memory will then be sent to the device only if the data consistency start signal (Y(n+1)A to Y(n+1)F) is switched to ON or when the output data consistency enable flag is OFF again.

NOTE

If just an CH☐ Output data consistency enable flag is set, the ME1IOL6-L will send the output data from the buffer memory to the device once – when the CH☐ Data consistency start signal (Y(n+1)A to Y(n+1)F) is being set to ON. This is to ensure, that the device will get the same data as in the buffer memory before the master signals "consistent data available".

4.3.7 Reading and Writing of Parameter Data

IO-Link defines service data to be exchangeable between an IO-Link device and the application. These parameters can be indexed from 2 to 32767 and may have a length of up to 232 bytes each (index 0 and 1 is for direct parameter page addressing). The exchange of service data happens in acyclic manner on user/application demand.

Request and answer area the buffer memory

To provide this functionality to the PLC, the IO-Link Master module offers two buffer memory areas for reading and writing those parameter record sets for each channel:

– The Acyclic Communication Request Data area (see section 4.5.14) and the

– Acyclic Communication Answer Data area (see section 4.5.17).

Both areas have some header information, followed by the parameter data. The detailed setup of the data areas is given in the following tables.

Item	Description		Setting range	Size (words)
Command	The type of access to a parameter (read/write).		100H to 102H 200H to 202H 301H	1
Index	Defines the parameter to access.		0 to 32767	1
Sub index	Defines the offset within the parameter.		0 to 231	1
Data size	The size in bytes of the data to be transferred.	Only required in case of a write request.	0 to 254	1
Data	The data to be transferred.		—	128

Tab. 4-10: *Data required for an acyclic communication request*

Item	Description		Setting range	Size (words)
Command	The type of access to a parameter (read/write).	The data sent in the request is returned.	100H to 102H 200H to 202H	1
Index	Defines the parameter to access.		0 to 32767	1
Sub index	Defines the offset within the parameter		0 to 231	1
Result*	The result of the transaction		0000H to FFFFH	1
Data size*	The size in bytes of the data that was transferred.		0 to 254	1
Data*	The data that was transferred (in case of a read request).		—	128

Tab. 4-11: *Data store in the acyclic communication answer areas*

* If an acyclic transaction request has failed, the result area will contain an error code.

Exchange of data with an IO-Link device

A certain parameter is read from an IO-Link device by the following sequence:

① The sequence program writes the required data to the acyclic communication request data area of the corresponding channel, consisting of command, parameter index and sub index.

② The sequence program sets the corresponding acyclic communication request flag for the channel in the buffer memory address Un\G1280 (see section 4.5.15).

③ The IO-Link Master module performs the transfer and writes a result code into the acyclic communication answer area. In case of a read request, the response data and the data size will be stored also into this area.

According to the status of the communication, the ME1IOL6-L sets the corresponding acyclic communication response flags in the buffer memory address Un\G1281 (see section 4.5.16).

The dependency of the signals and the flags is shown in the following figure.

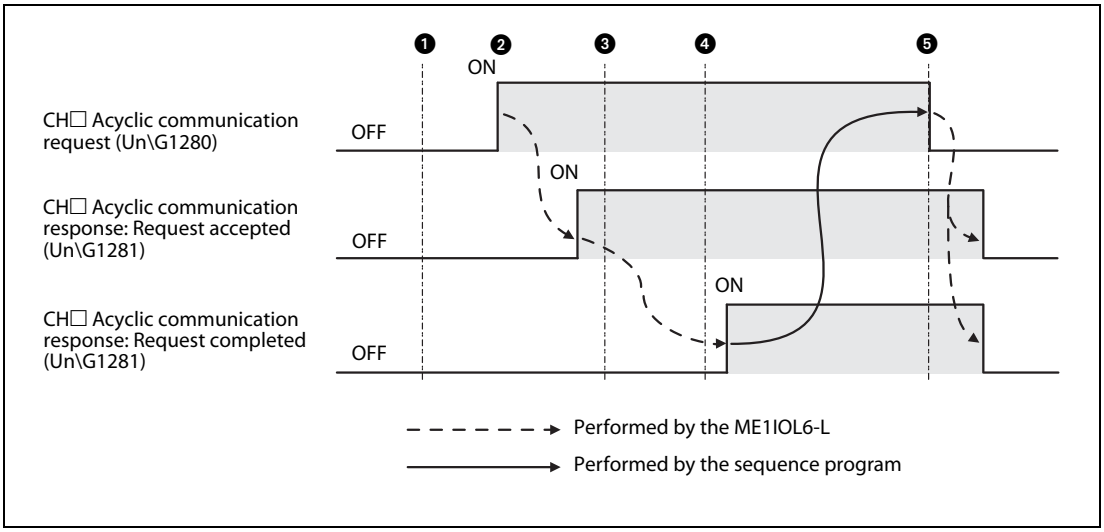


Fig. 4-6: *Timing of an acyclic communication request*

Number	Description
❶	The PLC sets the request data: command, index, etc
❷	The acyclic communication request for the corresponding channel is set.
❸	The request is forwarded to the IO-Link device.
❹	The IO-Link device responds to the request.
❺	The PLC reads the answer and resets the request flag.

Tab. 4-12: *Explanation for the timing shown above*

The process of writing a certain parameter to an IO-Link device is done accordingly:

① The sequence program writes the required data to the acyclic communication request data area of the corresponding channel, consisting of command, parameter index, sub index and data size.

② The sequence program writes the parameter data to the acyclic communication request data area.

③ The sequence program sets the corresponding acyclic communication request flag for the channel in the buffer memory address Un\G1280 (see section 4.5.15).

④ The IO-Link Master module performs the transfer to the device and writes a result code into the acyclic communication answer area. In case of a write request, there will be no more data than the result code in this area.

According to the status of the communication, the ME1IOL6-L sets the corresponding acyclic communication response flags in the buffer memory address Un\G1281 (see section 4.5.16).

NOTE

The execution of an acyclic communication request is secured by a time-out of 60 seconds.
If within that time no response is given by the IO-Link device, the execution will be aborted. The request completed flag will be set and the acyclic communication result area shows 1100H indicating the timeout.

4.3.8 Direct Parameter Page

Direct parameter page 1 (DPP1) read access

The data of parameter page 1 can be accessed by the acyclic communication function (refer to section 4.3.7) but for easier handling is also directly mapped into the buffer memory.

For each channel a direct parameter page 1 read area is reserved in the buffer memory. The IO-Link master module reads the page from the IO-Link device and stores the 16 bytes of parameter data into the buffer memory area. A read access is initiated by setting the direct parameter page 1 (DPP1) read request flag.

The direct parameter page 1 (DPP1) read response flag indicates that data is available in the buffer memory.

For a detailed information of reading the direct parameter page 1 please refer to section 4.5.18.

Direct parameter page 1 (DPP1) write access

A write access to direct parameter page 1 is not supported.

4.3.9 Automatic Confirmation of Events

By sending event data to the IO-Link master, an IO-Link device can inform about warnings, errors, etc. The ME1IOL6-L will store these events into the buffer memory.

Some of the event types can be set to be "ignored". The ME1IOL6-L will confirm these events automatically. The type of events to ignore can be set in the event auto confirmation setting (Un\G320 to Un\G325).

For a detailed description of the event handling and the automatic confirmation of events, please refer to section 4.5.13.

4.3.10 Data Storage

The data storage function is a feature of IO-Link V1.1, which is only available if the connected IO-Link device supports this function. By default the data storage function is disabled.

The data storage function can be enabled by setting the appropriate bits in the buffer memory address for data storage setting (Un\G255). The user can select whether upload or download of data is enabled.

The enabling/disabling of the data storage function is described in section 4.5.8.

Upload and download of data from/to IO-Link devices and deletion of stored data

Precondition for upload is an empty data storage or compatible device data. Download is only executed if the connected device is compatible.

To trigger the data exchange between the data storage and an IO-Link device, the sequence program has to use the acyclic communication function (see section 4.3.7).

The acyclic communication command code for accessing data storage is 202H. Depending on the given index, different commands can be triggered.

The following table shows the data required in the acyclic communication request area in the buffer memory.

Item	Contents	Meaning	Description
Command	202H	Data storage	Code for accessing data storage
Index	1H	Upload	Upload of parameter from IO-Link device to data storage
	2H	Download	Download of parameter from data storage to IO-Link device
	3H	Clear	Clear parameter data in data storage.
Sub index	—	—	Not used
Data size	—	—	
Data	—	—	

Tab. 4-13: *Data required for an acyclic communication request related to data storage*

The execution of the command is requested by the acyclic communication execution flag (section 4.5.15) and the result will be reflected by the acyclic communication response flag (section 4.5.16).

When the execution of the request has been completed, the result will be stored in the acyclic communication answer area (see section 4.5.17). Possible values are shown in the following table.

Result (hexadecimal)	Meaning
0000H	The operation was successful.
0001H	Operation failed (state conflict)
E0FFH	Invalid index, data storage is disabled

Tab. 4-14: *Acyclic communication request results for upload/download/deletion*

According to the acyclic communication specification, the command code and the index value will be reflected to the answer data area. The buffer memory addresses for the sub index, the data size as well as the data area will not contain valid data when the function returns.

Read/Write backup of data storage

Backup of data storage data is done by use of the acyclic communication. A total of 2048 bytes of parameter data can be exchanged with the data storage. Since the buffer memory area for acyclic communication is limited to 256 bytes, the data has to be exchanged with subsequent calls, using the data size and the index values.

NOTE

In case of reading/writing data with sizes exceeding 256 bytes only one channel at a time can be accessed.

- Reading of data from the data storage to the buffer memory

  The command code for reading data from the data storage to the buffer memory is 200H.

  The use of index 0 will start the exchange process for the whole 2048 bytes. This means that for reading the data from the master into the buffer memory, the application has to start with a read command with index 0. The command will return after receiving all the data from the data storage and will present the first 256 byte in the acyclic communication answer area. Further reads with indices 1 to 7 will then return the parameter data from byte 256 to 2048. The data size will contain the actual amount of data in that index.

NOTE

The application can skip further reads on higher indices if the current one returned with a data size that is smaller than 256. In this case, the rest of the parameter data is empty.

- Writing of data from the buffer memory to the data storage

  The command code for writing data from the buffer memory to the data storage is 201H.

  For writing the data to the data storage, the application should first fill the masters internal buffer with the data referred by indices 1 to 7 and finally set the first 256 bytes by use of index 0: The transfer process will start.

4.3.11 Device Validation

When the device validation is activated the ME1IOL6-L checks the connected IO-Link device at every start-up of the IO-Link communication. In case that the validation is not successful a device error is indicated by the ME1IOL6-L.

The device validation can be set using the acyclic communication (refer to section 4.3.7).

Two types of validation are selectable:

– Compatible device

  The newly connected device must have the same vendor ID and IO-Link Device ID as the configured device. With this setting, it is possible to replace a broken device by another device of the same type.

– Identical device

  The newly connected device must have the same vendor ID, IO-Link Device ID and serial number as the confederated device. In other words, the same device must be connected again.

NOTE

The validation setting must be executed
– after every PLC reset or
– after every power-on of the PLC.

The following table shows the data required in the acyclic communication request area in the buffer memory.

Item	Contents	Meaning	Description
Command	301H	Device validation	Code for device validation (write request)
Index	0H	Validation type	Validation deactivated
	1H		Validation of vendor ID and IO-Link Device ID (compatible)
	2H		Validation of vendor ID, IO-Link Device ID and serial number (identical)
Sub index	—	—	—
Data size	—	—	—
Data	see table below	—	Device data

Tab. 4-15: *Data required for an acyclic communication request for device validation*

The following table shows the arrangement of the data in the buffer memory.

Buffer memory address*		Meaning	
Hexadecimal	**Decimal**	**High byte**	**Low byte**
BFMH + 0000H	BFM + 0	Vendor ID 1 (MSB)	Vendor ID 2 (LSB)
BFMH + 0001H	BFM + 1	Device ID 1 (MSB)	Device ID 2
BFMH + 0002H	BFM + 2	Device ID 3 (LSB)	Serial number 1
BFMH + 0003H	BFM + 3	Serial number 2	Serial number 3
BFMH + 0004H	BFM + 4	Serial number 4	Serial number 5
BFMH + 0005H	BFM + 5	Serial number 6	Serial number 7
BFMH + 0006H	BFM + 6	Serial number 8	Serial number 9
BFMH + 0007H	BFM + 7	Serial number 10	Serial number 11
BFMH + 0008H	BFM + 8	Serial number 12	Serial number 13
BFMH + 0009H	BFM + 9	Serial number 14	Serial number 15
BFMH + 000AH	BFM + 10	Serial number 16	Reserved (Fixed to 0.)

Tab. 4-16: *Storage of device data in the buffer memory*

* To obtain the actual address, add the start address for the request data area of the corresponding channel. For example, the Device ID 1 and the Device ID 2 of the device connected to channel 1 can be found in the address Un\G420 + 1 = Un\G421.

The execution of the command is requested by the acyclic communication execution flag (section 4.5.15) and the result will be reflected by the acyclic communication response flag (section 4.5.16).

When the execution of the request has been completed, the result will be stored in the acyclic communication answer area (see section 4.5.17). Possible values are shown in the following table.

Result (hexadecimal)	Meaning
0000_H	The operation was successful.
0001_H	Operation failed (state conflict)

Tab. 4-17: *Acyclic communication request results for device validation*

According to the acyclic communication specification, the command code and the index value will be reflected to the answer data area. The buffer memory addresses for the sub index, the data size as well as the data area will not contain valid data when the function returns.

4.4 I/O Signals for the Programmable Controller CPU

4.4.1 List of I/O signals

Note that the I/O numbers (X/Y) shown in this section and thereafter depends on the mounting position resp. on the start I/O number or head address of the IO-Link master module. This head address has to be added to the shown I/O numbers.

For example, if the IO-Link master module occupies the range from X/Y040 to Y/X05F the head address is X/Y040. However the least significant digit is omitted and the head address "n" in this case reads as "4". The "module ready" input (Xn0) will be X40 and the "event flag" will be X50.

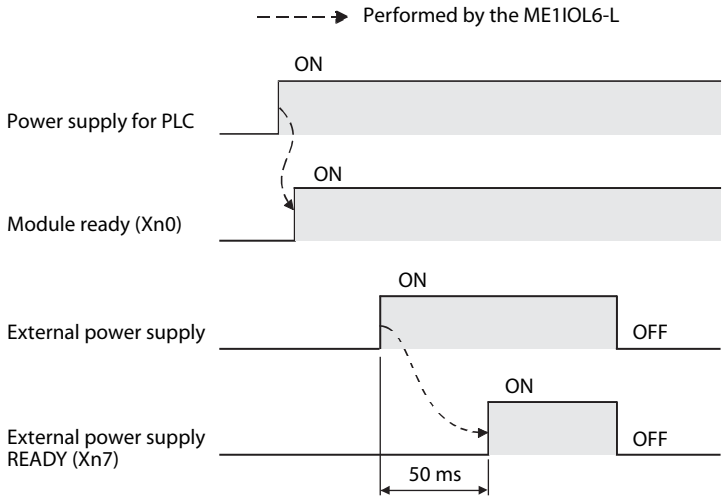
Signal direction CPU Module ← ME1IOL6-L				Signal direction CPU Module → ME1IOL6-L			
Device No. (Input)	**Signal name**		**Reference**	**Device No. (Output)**	**Signal name**		**Reference**
Xn0	Module ready		Section 4.4.2	Yn0	Use prohibited		Section 4.4.3
Xn1	CH1	• Digital input (SIO mode) • Data mask result (IO-Link mode)		Yn1	CH1	Digital output (SIO mode)	
Xn2	CH2			Yn2	CH2		
Xn3	CH3			Yn3	CH3		
Xn4	CH4			Yn4	CH4		
Xn5	CH5			Yn5	CH5		
Xn6	CH6			Yn6	CH6		
Xn7	External power (24 V DC) ready			Yn7	Use prohibited		—
Xn8	Use prohibited		—	Yn8			
Xn9				Yn9			
XnA				YnA			
XnB				YnB			
XnC				YnC			
XnD				YnD			
XnE				YnE			
XnF	Error flag		Section 4.4.2	YnF			
X(n+1)0	Event flag			Y(n+1)0			
X(n+1)1	CH1	Input data invalid		Y(n+1)1	CH1	Output data valid	Section 4.4.3
X(n+1)2	CH2			Y(n+1)2	CH2		
X(n+1)3	CH3			Y(n+1)3	CH3		
X(n+1)4	CH4			Y(n+1)4	CH4		
X(n+1)5	CH5			Y(n+1)5	CH5		
X(n+1)6	CH6			Y(n+1)6	CH6		
X(n+1)7	Use prohibited		—	Y(n+1)7	Use prohibited		—
X(n+1)8				Y(n+1)8			
X(n+1)9				Y(n+1)9			
X(n+1)A	CH1	Consistent data available	Section 4.4.2	Y(n+1)A	CH1	Data consistency start	Section 4.4.3
X(n+1)B	CH2			Y(n+1)B	CH2		
X(n+1)C	CH3			Y(n+1)C	CH3		
X(n+1)D	CH4			Y(n+1)D	CH4		
X(n+1)E	CH5			Y(n+1)E	CH5		
X(n+1)F	Ch6			Y(n+1)F	CH6		

Tab. 4-18: *I/O signals of the ME1IOL6-L*

NOTE

The "Use prohibited" signals cannot be used by the user since they are for system use only.
If these signals are turned ON/OFF by the sequence program, the performance of the IO-Link master module cannot be guaranteed.

4.4.2 Details of Input Signals

Device No.	Signal Name	Description
Xn0	Module ready	• When the programmable controller CPU is powered on or reset, this signal turns on once the module has finished internal initialization. • When a watchdog timer error occurs, "Module ready" (X0) turns OFF.
Xn1 to Xn6	CH□ digital input (SIO mode)	The digital input value of the corresponding channel is reflected. • The signal is ON when the channel's input is logical high. • The signal is OFF when the channel's input is logical low. These signal values are only valid if the external 24V supply voltage is in the specified input range.
	CH□ data mask result (IO-Link mode)	This signal represents the result of the input process data combined with the input data mask, defined by the user (refer to section 4.3.3).
Xn7	External power supply READY	The state of the external power supply (24 V DC) is shown by signal Xn7: • The signal turns ON, 50 ms after the external power supply is turned on. • The signal turns OFF immediately after a loss of the external power supply is detected. • The following diagram shows the timing of this signal. 
XnF	Error flag	• The error flag turns ON when one of the channel error flags or the module error flag turns ON. • To turn the error flag (XnF) OFF, remove the cause of the error and confirm the error by setting the related error reset flag in buffer memory.
X(n+1)0	Event flag	• The event flag turns ON when one of the channels announces a new event. • The signal turns OFF when no un-confirmed event is pending.
X(n+1)1 to X(n+1)6	CH□ input data invalid	• The channel input data invalid flag turns ON when input data (IO-Link or SIO mode) is not updated any more. • The channel input data invalid flag turns ON when input data is marked as invalid by the IO-Link device (IO-Link mode).
X(n+1)A to X(n+1)F	CH□ consistent data available	• In case of consistent process data access the module indicates that the process data area in the buffer memory can be accessed. It is not updated until the "Data consistency start signal" (Y(n+1)A to Y(n+1)F) is reset by the user.

Tab. 4-19: *Detailed description of the input signals (Signal direction ME1IOL6-L → CPU Module)*

4.4.3 Details of Output Signals

Device No.	Signal Name	Description
Yn1 to Yn6	CH□ digital output (SIO mode)	Digital output signal in SIO mode.
Y(n+1)1 to Y(n+1)6	CH□ output data valid	Set this signal to ON to set the output data of the corresponding channel valid. The logical output level of the channel will stay low as long as the Channel output data valid flag is OFF. NOTE: The IO-Link master will only forward this signal to the IO-Link device if it comprises output data.
Y(n+1)A to Y(n+1)F	CH□ data consistency start	Set this signal to exchange more than 1 word of input/ output process data in consistent manner. The module will then stop updating the input area and reading the output area for that channel and turn ON X(n+1)A to X(n+1)F to indicate consistent access available. When finished accessing the buffer memory, reset Y(n+1)A to Y(n+1)F to allow data transfer. Set the "Output Data Consistency Enable Flag" also to ON to get consistent output process data. For more details on consistent data exchange, please refer to section 4.3.6.

Tab. 4-20: *Detailed description of the output signals (Signal direction CPU Module → ME1IOL6-L)*

4.5 Buffer Memory

The ME1IOL6-L has a memory range assigned as a buffer for temporary storage of data, such as process data or error information. The PLC CPU can access this buffer and both read the stored values from it and write new values to it which the module can then process (output values, settings for the function of the IO-Link devices etc).

Each buffer memory address consists of 16 bits.

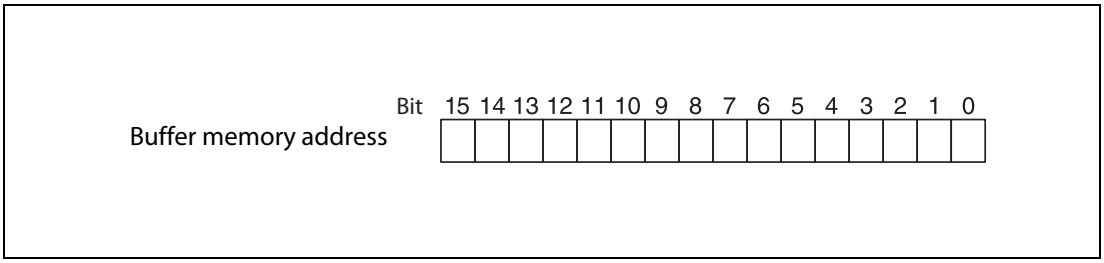


Fig. 4-7: *Assignments of bits to a buffer memory address*

NOTE

Do not write data in the "system areas" of the buffer memory. If data is written to any of the system areas, the PLC system may not be operated properly. Some of the user areas contain partially system areas. Care must be taken when reading/writing to the buffer memory.
Also, do not write data (e.g. in a sequence program) to the buffer memory area where writing is disabled. Doing so may cause malfunction.

The "Default" value indicated in the following tables is the initial value set after the power is turned on or the PLC CPU is reset.

Instructions for data exchange with the buffer memory

Communication between the PLC CPU and the buffer memory of special function modules is performed with FROM and TO instructions. The buffer memory of a special function module can also accessed directly, e. g. with a MOV instruction.

Format of the device address: Un\Gn

– Un: Head address of the special function module

– Gn: Buffer memory address (decimal)

For example the device address U3\G11designates the buffer memory address 11 in the special function module with the head address 3 (X/Y30 to X/Y3F).

In this User's Manual the latter form of addressing is used widely.

For full documentation of all the instructions used with examples please refer to the Programming Manual for the MELSEC System Q and the MELSEC-L series.

4.5.1 Buffer memory assignment

Address		Description		Default	R/W*	Reference
Hexa-decimal	Decimal					
0H	0	CH1	Input process data in IO-Link mode	0000H	R	Section 4.5.2
to	to					
FH	15					
10H	16	CH2	Input process data in IO-Link mode	0000H	R	
to	to					
1FH	31					
20H	32	CH3	Input process data in IO-Link mode	0000H	R	
to	to					
2FH	47					
30H	48	CH4	Input process data in IO-Link mode	0000H	R	
to	to					
3FH	63					
40H	64	CH5	Input process data in IO-Link mode	0000H	R	
to	to					
4FH	79					
50H	80	CH6	Input process data in IO-Link mode	0000H	R	
to	to					
5FH	95					
60H	96	System area		—	—	—
to	to					
6FH	111					
70H	112	CH1	Output process data in IO-Link mode	0000H	R/W	Section 4.5.3
to	to					
7FH	127					
80H	128	CH2	Output process data in IO-Link mode	0000H	R/W	
to	to					
8FH	143					
90H	144	CH3	Output process data in IO-Link mode	0000H	R/W	
to	to					
9FH	159					
A0H	160	CH4	Output process data in IO-Link mode	0000H	R/W	
to	to					
AFH	175					
B0H	176	CH5	Output process data in IO-Link mode	0000H	R/W	
to	to					
BFH	191					
C0H	192	CH6	Output process data in IO-Link mode	0000H	R/W	
to	to					
CFH	207					
D0H	208	System area		—	—	—
to	to					
DFH	223					
E0H	224	CH1	Input data mask	0000H	R/W	Section 4.5.4
E1H	225	CH2		0000H	R/W	
E2H	226	CH3		0000H	R/W	
E3H	227	CH4		0000H	R/W	
E4H	228	CH5		0000H	R/W	
E5H	229	CH6		0000H	R/W	

Tab. 4-21: *Buffer memory assignment of the ME1IOL6-L (1/9)*

* Indicates whether reading from and writing to a sequence program are enabled.
R : Read enabled
W : Write enabled

Address		Description		Default	R/W*	Reference
Hexa-decimal	Decimal					
E6H	230	Output data consistency enable		0000H	R/W	Section 4.5.5
E7H	231	System area		—	—	—
to	to					
EFH	239					
F0H	240	Channel mode change flag		0000H	R/W	Section 4.5.6
F1H	241	Channel mode change complete		0000H	R	
F2H	242	CH1	Mode change result	0000H	R	
F3H	243	CH2		0000H	R	
F4H	244	CH3		0000H	R	
F5H	245	CH4		0000H	R	
F6H	246	CH5		0000H	R	
F7H	247	CH6		0000H	R	
F8H	248	CH1	Mode setting	0000H	R/W	
F9H	249	CH2		0000H	R/W	
FAH	250	CH3		0000H	R/W	
FBH	251	CH4		0000H	R/W	
FCH	252	CH5		0000H	R/W	
FDH	253	CH6		0000H	R/W	
FEH	254	System area		—	—	—
FFH	255	Data storage setting		0000H	R/W	Section 4.5.8
100H	256	System area		—	—	—
to	to					
10FH	271					
110H	272	CH1	Current mode	0000H	R	Section 4.5.8
111H	273	CH2		0000H	R	
112H	274	CH3		0000H	R	
113H	275	CH4		0000H	R	
114H	276	CH5		0000H	R	
115H	277	CH6		0000H	R	
116H	278	System area		—	—	—
117H	279	Current data storage setting		0000H	R	Section 4.5.9
118H	280	Channel error flag		0000H	R	Section 4.5.10
119H	281	Channel error reset flag		0000H	R/W	
11AH	282	Module diagnostic information		0000H	R	Section 4.5.11
11BH	283	CH1	Diagnostic information	0000H	R	Section 4.5.12
11CH	284	CH2		0000H	R	
11DH	285	CH3		0000H	R	
11EH	286	CH4		0000H	R	
11FH	287	CH5		0000H	R	
120H	288	CH6		0000H	R	
121H	289	System area		—	—	—
to	to					
13EH	318					
13FH	319					

Tab. 4-22: *Buffer memory assignment of the ME1IOL6-L (2/9)*

* Indicates whether reading from and writing to a sequence program are enabled.
R : Read enabled
W : Write enabled

Address		Description		Default	R/W*	Reference
Hexa-decimal	Decimal					
140H	320	CH1	Event Auto Confirmation Setting	0000H	R/W	Section 4.5.13
141H	321	CH2		0000H	R/W	
142H	322	CH3		0000H	R/W	
143H	323	CH4		0000H	R/W	
144H	324	CH5		0000H	R/W	
145H	325	CH6		0000H	R/W	
146H	326	Event reset flag		0000H	R/W	
147H	327	Event flag		0000H	R	
148H	328	CH1	Event ID	0000H	R	Section 4.5.13
149H	329		Event Qualifier	0000H	R	
14AH	330		Event Code	0000H	R	
14BH	331	System area		—	—	—
to	to					
14FH	335					
150H	336	CH2	Event ID	0000H	R	Section 4.5.13
151H	337		Event Qualifier	0000H	R	
152H	338		Event Code	0000H	R	
153H	339	System area		—	—	—
to	to					
157H	343					
158H	344	CH3	Event ID	0000H	R	Section 4.5.13
159H	345		Event Qualifier	0000H	R	
15AH	346		Event Code	0000H	R	
15BH	347	System area		—	—	—
to	to					
15FH	351					
160H	352	CH4	Event ID	0000H	R	Section 4.5.13
161H	353		Event Qualifier	0000H	R	
162H	354		Event Code	0000H	R	
163H	355	System area		—	—	—
to	to					
167H	359					
168H	360	CH5	Event ID	0000H	R	Section 4.5.13
169H	361		Event Qualifier	0000H	R	
16AH	362		Event Code	0000H	R	
16BH	363	System area		—	—	—
to	to					
16FH	367					
170H	368	CH6	Event ID	0000H	R	Section 4.5.13
171H	369		Event Qualifier	0000H	R	
172H	370		Event Code	0000H	R	
173H	371	System area		—	—	—
to	to					
19FH	415					

Tab. 4-23: *Buffer memory assignment of the ME1IOL6-L (3/9)*

* Indicates whether reading from and writing to a sequence program are enabled.
R : Read enabled
W : Write enabled

Address		Description			Default	R/W*	Reference
Hexa-decimal	Decimal						
1A0H	416	CH1	Acyclic communication request	Command	0000H	R/W	Section 4.5.14
1A1H	417			Index	0000H	R/W	
1A2H	418			Sub index	0000H	R/W	
1A3H	419			Data size	0000H	R/W	
1A4H	420			Data (128 words)	0000H	R/W	
to	to						
223H	547						
224H	548	System area			—	—	—
to	to						
22FH	559						
230H	560	CH2	Acyclic communication request	Command	0000H	R/W	Section 4.5.14
231H	561			Index	0000H	R/W	
232H	562			Sub index	0000H	R/W	
233H	563			Data size	0000H	R/W	
234H	564			Data (128 words)	0000H	R/W	
to	to						
2B3H	691						
2B4H	692	System area			—	—	—
to	to						
2BFH	703						
2C0H	704	CH3	Acyclic communication request	Command	0000H	R/W	Section 4.5.14
2C1H	705			Index	0000H	R/W	
2C2H	706			Sub index	0000H	R/W	
2C3H	707			Data size	0000H	R/W	
2C4H	708			Data (128 words)	0000H	R/W	
to	to						
343H	835						
344H	836	System area			—	—	—
to	to						
34FH	847						
350H	848	CH4	Acyclic communication request	Command	0000H	R/W	Section 4.5.14
351H	849			Index	0000H	R/W	
352H	850			Sub index	0000H	R/W	
353H	851			Data size	0000H	R/W	
354H	852			Data (128 words)	0000H	R/W	
to	to						
3D3H	979						
3D4H	980	System area			—	—	—
to	to						
3DFH	991						
3E0H	992	CH5	Acyclic communication request	Command	0000H	R/W	Section 4.5.14
3E1H	993			Index	0000H	R/W	
3E2H	994			Sub index	0000H	R/W	
3E3H	995			Data size	0000H	R/W	
3E4H	996			Data (128 words)	0000H	R/W	
to	to						
463H	1123						
464H	1124	System area			—	—	—
to	to						
46FH	1135						

Tab. 4-24: *Buffer memory assignment of the ME1IOL6-L (4/9)*

* Indicates whether reading from and writing to a sequence program are enabled.
R : Read enabled
W : Write enabled

Address		Description			Default	R/W*	Reference
Hexa-decimal	Decimal						
470H	1136	CH6	Acyclic communication request	Command	0000H	R/W	Section 4.5.14
471H	1137			Index	0000H	R/W	
472H	1138			Sub index	0000H	R/W	
473H	1139			Data size	0000H	R/W	
474H	1140			Data (128 words)	0000H	R/W	
to	to						
4F3H	1267						
4F4H	1268	System area			—	—	—
to	to						
4FFH	1279						
500H	1280	Acyclic communication		Request flag	0000H	R/W	Section 4.5.15
501H	1281			Response flag	0000H	R	Section 4.5.16
502H	1282	System area			—	—	—
to	to						
50FH	1295						
510H	1296	CH1	Acyclic communication answer	Command	0000H	R	Section 4.5.17
511H	1297			Index	0000H	R	
512H	1298			Sub index	0000H	R	
513H	1299			Result	0000H	R	
514H	1300			Data size	0000H	R	
515H	1301			Data (128 words)	0000H	R	
to	to						
594H	1428						
595H	1429	System area			—	—	—
to	to						
59FH	1439						
5A0H	1440	CH2	Acyclic communication answer	Command	0000H	R	Section 4.5.17
5A1H	1441			Index	0000H	R	
5A2H	1442			Sub index	0000H	R	
5A3H	1443			Result	0000H	R	
5A4H	1444			Data size	0000H	R	
5A5H	1445			Data (128 words)	0000H	R	
to	to						
624H	1572						
625H	1573	System area			—	—	—
to	to						
62FH	1583						
630H	1584	CH3	Acyclic communication answer	Command	0000H	R	Section 4.5.17
631H	1585			Index	0000H	R	
632H	1586			Sub index	0000H	R	
633H	1587			Result	0000H	R	
634H	1588			Data size	0000H	R	
635H	1589			Data (128 words)	0000H	R	
to	to						
6B4H	1716						
6B5H	1717	System area			—	—	—
to	to						
6BFH	1727						

Tab. 4-25: *Buffer memory assignment of the ME1IOL6-L (5/9)*

* Indicates whether reading from and writing to a sequence program are enabled.
R : Read enabled
W : Write enabled

Address		Description			Default	R/W*	Reference
Hexa-decimal	Decimal						
6C0H	1728	CH4	Acyclic communication answer	Command	0000H	R	Section 4.5.17
6C1H	1729			Index	0000H	R	
6C2H	1730			Sub index	0000H	R	
6C3H	1731			Result	0000H	R	
6C4H	1732			Data size	0000H	R	
6C5H	1733			Data (128 words)	0000H	R	
to	to						
744H	1860						
745H	1861	System area			—	—	—
to	to						
74FH	1871						
750H	1872	CH5	Acyclic communication answer	Command	0000H	R	Section 4.5.17
751H	1873			Index	0000H	R	
752H	1874			Sub index	0000H	R	
753H	1875			Result	0000H	R	
754H	1876			Data size	0000H	R	
755H	1877			Data (128 words)	0000H	R	
to	to						
7D4H	2004						
7D5H	2005	System area			—	—	—
to	to						
7DFH	2015						
7E0H	2016	CH6	Acyclic communication answer	Command	0000H	R	Section 4.5.17
7E1H	2017			Index	0000H	R	
7E2H	2018			Sub index	0000H	R	
7E3H	2019			Result	0000H	R	
7E4H	2020			Data size	0000H	R	
7E5H	2021			Data (128 words)	0000H	R	
to	to						
864H	2148						
865H	2149	System area			—	—	—
to	to						
86DH	2157						

Tab. 4-26: *Buffer memory assignment of the ME1IOL6-L (6/9)*

* Indicates whether reading from and writing to a sequence program are enabled.
R : Read enabled
W : Write enabled

Address		Description				Default	R/W*	Reference
Hexa-decimal	Decimal							
86EH	2158	Direct parameter page 1 (DPP1)		Read request flag		0000H	R/W	Section 4.5.18
86FH	2159			Read response flag		0000H	R	
870H	2160	CH1	Direct parameter page 1 (DPP1)	High byte	Low byte	0000H	R	Section 4.5.18
				Master Cycle Time (Address 01H)	Master Command (Address 00H)			
871H	2161			F-sequence Capability (Address 03H)	Min. Cycle Time (Address 02H)	0000H	R	
872H	2162			Process Data In (Address 05H)	IO-Link Revision ID (Address 04H)	0000H	R	
873H	2163			Vendor ID 1 (MSB) (Address 07H)	Process Data Out (Address 06H)	0000H	R	
874H	2164			Device ID 1 (MSB) (Address 09H)	Vendor ID 2 (LSB) (Address 08H)	0000H	R	
875H	2165			Device ID 3 (LSB) (Address 0BH)	Device ID 2 (Address 0AH)	0000H	R	
876H	2166			Function ID (high) (Address 0DH)	Function ID (low) (Address 0CH)	0000H	R	
877H	2167			System Command (Address 0FH)	Reserved (Address 0EH)	0000H	R	
878H	2168	System area				—	—	—
to	to							
87FH	2175							
880H	2176	CH2	Direct parameter page 1 (DPP1)	High byte	Low byte	0000H	R	Section 4.5.18
				Master Cycle Time (Address 01H)	Master Command (Address 00H)			
881H	2177			F-sequence Capability (Address 03H)	Min. Cycle Time (Address 02H)	0000H	R	
882H	2178			Process Data In (Address 05H)	IO-Link Revision ID (Address 04H)	0000H	R	
883H	2179			Vendor ID 1 (MSB) (Address 07H)	Process Data Out (Address 06H)	0000H	R	
884H	2180			Device ID 1 (MSB) (Address 09H)	Vendor ID 2 (LSB) (Address 08H)	0000H	R	
885H	2181			Device ID 3 (LSB) (Address 0BH)	Device ID 2 (Address 0AH)	0000H	R	
886H	2182			Function ID (high) (Address 0DH)	Function ID (low) (Address 0CH)	0000H	R	
887H	2183			System Command (Address 0FH)	Reserved (Address 0EH)	0000H	R	
888H	2184	System area				—	—	—
to	to							
88FH	2191							

Tab. 4-27: *Buffer memory assignment of the ME1IOL6-L (7/9)*

* Indicates whether reading from and writing to a sequence program are enabled.
R : Read enabled
W : Write enabled

Address		Description				Default	R/W*	Reference
Hexa-decimal	Decimal							
890H	2192	CH3	Direct parameter page 1 (DPP1)	High byte: Master Cycle Time (Address 01H)	Low byte: Master Command (Address 00H)	0000H	R	Section 4.5.18
891H	2193			F-sequence Capability (Address 03H)	Min. Cycle Time (Address 02H)	0000H	R	
892H	2194			Process Data In (Address 05H)	IO-Link Revision ID (Address 04H)	0000H	R	
893H	2195			Vendor ID 1 (MSB) (Address 07H)	Process Data Out (Address 06H)	0000H	R	
894H	2196			Device ID 1 (MSB) (Address 09H)	Vendor ID 2 (LSB) (Address 08H)	0000H	R	
895H	2197			Device ID 3 (LSB) (Address 0BH)	Device ID 2 (Address 0AH)	0000H	R	
896H	2198			Function ID (high) (Address 0DH)	Function ID (low) (Address 0CH)	0000H	R	
897H	2199			System Command (Address 0FH)	Reserved (Address 0EH)	0000H	R	
898H	2200	System area				—	—	—
to	to							
89FH	2207							
8A0H	2208	CH4	Direct parameter page 1 (DPP1)	High byte: Master Cycle Time (Address 01H)	Low byte: Master Command (Address 00H)	0000H	R	Section 4.5.18
8A1H	2209			F-sequence Capability (Address 03H)	Min. Cycle Time (Address 02H)	0000H	R	
8A2H	2210			Process Data In (Address 05H)	IO-Link Revision ID (Address 04H)	0000H	R	
8A3H	2211			Vendor ID 1 (MSB) (Address 07H)	Process Data Out (Address 06H)	0000H	R	
8A4H	2212			Device ID 1 (MSB) (Address 09H)	Vendor ID 2 (LSB) (Address 08H)	0000H	R	
8A5H	2213			Device ID 3 (LSB) (Address 0BH)	Device ID 2 (Address 0AH)	0000H	R	
8A6H	2214			Function ID (high) (Address 0DH)	Function ID (low) (Address 0CH)	0000H	R	
8A7H	2215			System Command (Address 0FH)	Reserved (Address 0EH)	0000H	R	
8A8H	2216	System area				—	—	—

Tab. 4-28: *Buffer memory assignment of the ME1IOL6-L (8/9)*

* Indicates whether reading from and writing to a sequence program are enabled.
R : Read enabled
W : Write enabled

Address		Description				Default	R/W*	Reference
Hexa-decimal	Decimal							
8B0H	2224	CH5	Direct parameter page 1 (DPP1)	High byte	Low byte	0000H	R	Section 4.5.18
				Master Cycle Time (Address 01H)	Master Command (Address 00H)			
8B1H	2225			F-sequence Capability (Address 03H)	Min. Cycle Time (Address 02H)	0000H	R	
8B2H	2226			Process Data In (Address 05H)	IO-Link Revision ID (Address 04H)	0000H	R	
8B3H	2227			Vendor ID 1 (MSB) (Address 07H)	Process Data Out (Address 06H)	0000H	R	
8B4H	2228			Device ID 1 (MSB) (Address 09H)	Vendor ID 2 (LSB) (Address 08H)	0000H	R	
8B5H	2229			Device ID 3 (LSB) (Address 0BH)	Device ID 2 (Address 0AH)	0000H	R	
8B6H	2230			Function ID (high) (Address 0DH)	Function ID (low) (Address 0CH)	0000H	R	
8B7H	2231			System Command (Address 0FH)	Reserved (Address 0EH)	0000H	R	
8B8H	2232	System area				—	—	—
to	to							
8BFH	2239							
8C0H	2240	CH6	Direct parameter page 1 (DPP1)	High byte	Low byte	0000H	R	Section 4.5.18
				Master Cycle Time (Address 01H)	Master Command (Address 00H)			
8C1H	2241			F-sequence Capability (Address 03H)	Min. Cycle Time (Address 02H)	0000H	R	
8C2H	2242			Process Data In (Address 05H)	IO-Link Revision ID (Address 04H)	0000H	R	
8C3H	2243			Vendor ID 1 (MSB) (Address 07H)	Process Data Out (Address 06H)	0000H	R	
8C4H	2244			Device ID 1 (MSB) (Address 09H)	Vendor ID 2 (LSB) (Address 08H)	0000H	R	
8C5H	2245			Device ID 3 (LSB) (Address 0BH)	Device ID 2 (Address 0AH)	0000H	R	
8C6H	2246			Function ID (high) (Address 0DH)	Function ID (low) (Address 0CH)	0000H	R	
8C7H	2247			System Command (Address 0FH)	Reserved (Address 0EH)	0000H	R	
8C8H	2248	System area				—	—	—
to	to							
7FFFH	32767							

Tab. 4-29: *Buffer memory assignment of the ME1IOL6-L (9/9)*

* Indicates whether reading from and writing to a sequence program are enabled.
R : Read enabled
W : Write enabled

4.5.2 CH□ Input Process Data (Un\G0 to Un\G15, Un\G16 to Un\G31...)

In IO-Link mode, the area of input process data reflects the current data of the connected IO-Link device. Up to 32 bytes of input process data can be stored for each channel. The size and the structure of the data may vary for different IO-Link device types. For that reason, the ME1IOL6-L maps the data straight into the input process data area without any interpretation.

For the easy recognition of "high" bits in the first two bytes of the IO-Link process data the input process data bytes 1 and 2 are combined with the input data mask and form a resulting input signal for each channel (Xn1 to Xn6). For a detailed description of the input data mask, please refer to section 4.3.3.

The input process data area will be updated every time the connected IO-Link device announces new data to the master. Each channel's input process data area may be refreshed independently due to different cycle times of the channels.

NOTES

In IO-Link mode, the signal Xn□ of the channel will stay OFF if the input data mask is zero - even if the input process data is zero too

In case that IO-Link communication stops (e.g. due to under voltage, disconnection of an IO-Link device) the input process data buffer is set to 0.

4.5.3 CH□ Output Process Data (Un\G112 to Un\G127, Un\G128 to Un\G143...)

In IO-Link mode, the output process data stored in this area is output to the connected IO-Link device. The output data size may be up to 32 bytes for each channel. The size and the structure of the data may vary for different IO-Link device types and shall match the devices specification.

To write output data to the IO-Link device it is necessary to set the corresponding data valid signal Y(n+1)1 to Y(n+1)6 (refer to section 4.4).

In case of a PLC stop the output data is no longer refreshed in the buffer memory. The IO-Link device is notified by the output data valid signal (Y(n+1)1 to Y(n+1)6). The behaviour of the output data valid signals of the ME1IOL6-L can be defined by the intelligent function module switch no. 3 (refer to section 5.5.2).

4.5.4 CH□ Input Data Mask (Un\G224, Un\G225 to Un\G229)

The input data mask can be used to filter the input process data for parts of special attention. Two bytes are used to form that mask. The IO-Link master module will perform a bitwise AND operation between the mask and the first two bytes of CH□ input process data (refer to section 4.5.2). The result of that operation will be shown for each channel by the signals Xn1 to Xn6.

The CH□ input data mask is only active if their value is greater than 0.

For more information about the masking of input data, please refer to section 4.3.3.

4.5.5 Output Data Consistency Enable (Un\G230)

To request the writing of consistent output data, the user has to set the output data consistency enable flag for the corresponding channel. The output data from buffer memory will then be sent to the device only if the Data Consistency Start signal (Y(n+1)A to Y(n+1)F) is switched to ON or when the Output Data Consistency Enable flag is OFF again.

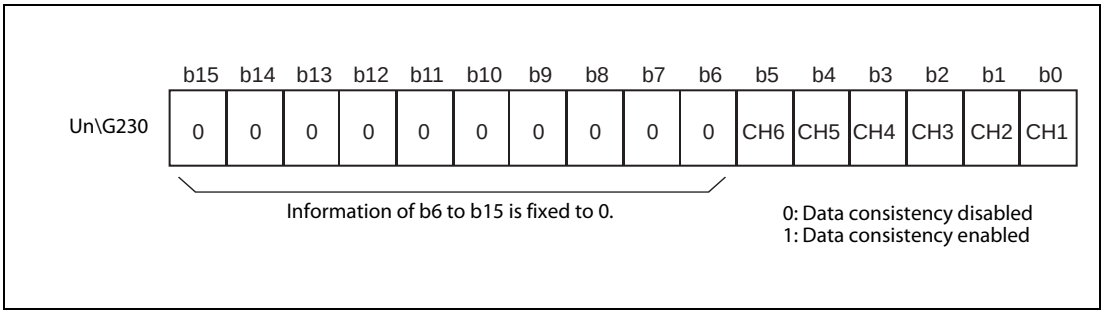


Fig. 4-8: *Assignment of the bits in buffer memory address 230*

NOTE

If just an Output Data Consistency Enable flag is set, the ME1IOL6-L will send the output data from the buffer memory to the device once – when the Data Consistency Start signal (Y(n+1)A to Y(n+1)F) is being set to ON. This is to ensure, that the device will get the same data as in the buffer memory before the master signals "consistent data available".

4.5.6 Changing the Channel Mode (Un\G240 to Un\G253)

At startup all channels of the ME1IOL6-L are deactivated. The sequence program can set the channels of the IO-Link master module to run in various modes or keep them deactivated.

The actual mode of each channel is shown in the buffer memory address for CH□ current mode (Un\G272 to Un\G277, section 4.5.7).

CH□ Channel Mode Settings (Un\G248, Un\G249...)

The setting of the target mode is done in the buffer memory address for CH□ channel mode setting (Un\G248 to Un\G253).

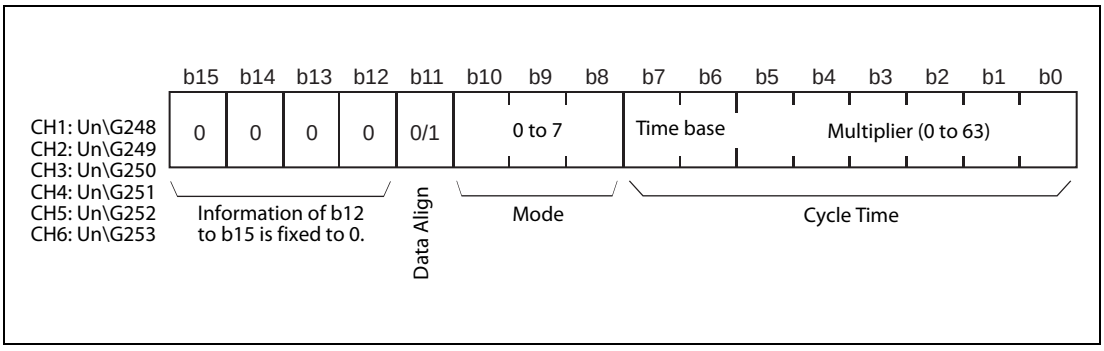


Fig. 4-9: *Assignment of the bits for the channel mode settings*

- Cycle time

  The low-byte of the mode setting, which defines the cycle time, is divided in the time base and a multiplier. The multiplier is a 6-bit factor for calculating the cycle time. Permissible values for the multiplier are 0 to 63.

  The permissible combinations for time base and multiplier are listed in the following table, along with the resulting values for the cycle time.

Time Base			Calculation	Cycle time
Binary code		Value		
b7	b6			
0	0	0.1 ms	Multiplier × Time Base	0.0 ms to 6.3 ms
0	1	0.4 ms	6.4 ms + Multiplier × Time Base	6.4 ms to 31.6 ms
1	0	1.6 ms	32.0 ms + Multiplier × Time Base	32.0 ms to 132.8 ms
1	1	—	Reserved	Reserved

Tab. 4-30: *Relation between time base, multiplier and cycle time*

  When the cycle time (bit 0 to bit 7) is set to "0" the master uses the fastest possible cycle time that is supported by the connected IO-Link device. The cycle time is only necessary when setting a port to IO-Link communication and should be left zero for any other mode setting.

- Mode

  The mode of the channel is defined by the bits b8 to b10. Possible values for the target mode are listed below.

Mode				Description	Signal setting	
Binary code			Value		L+□ (L+ line)	C□ (C/Q line)
b10	b9	b8				
0	0	0	0	Channel is deactivated	OFF	OFF
0	0	1	1	IO-Link mode	ON	Active
0	1	0	2	Reserved	—	—
0	1	1	3	Digital input mode (SIO mode)	ON	Active
1	0	0	4	Digital output mode (SIO mode)	ON	Active
1	0	1	5	Reserved	—	—
1	1	0	6			
1	1	1	7			

Tab. 4-31: *Setting of modes*

- Data align

  Bit 11 (Data align) controls the byte order of the device data in buffer memory.

  By default (Data align = 0 = Data swapping active), the byte order will be swapped.

  If Data align is set to 1, the swapping is disabled and the byte order of the data bytes in buffer memory will be the same as coming from the device.

  For a detailed description of the data swapping function please refer to section 4.3.5.

NOTE Cycle time and data align setting is only possible together with setting the IO-Link mode. During IO-Link operation no change is possible.

Channel Mode Change Flag (Un\G240)

To trigger the mode changing for one of the channels of the ME1IOL6-L, the user has to set the corresponding bit in Un\G240.

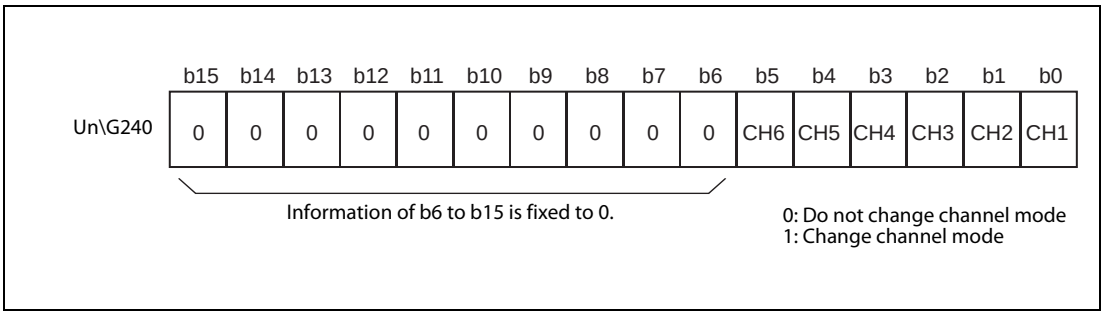


Fig. 4-10: *Assignment of the channel mode change flags*

Channel Mode Change Complete Flag (Un\G241)

After the mode changing has been triggered by a bit in Un\G240, the IO-Link device sets the corresponding bit in Un\G241 to show that the mode change has been completed.

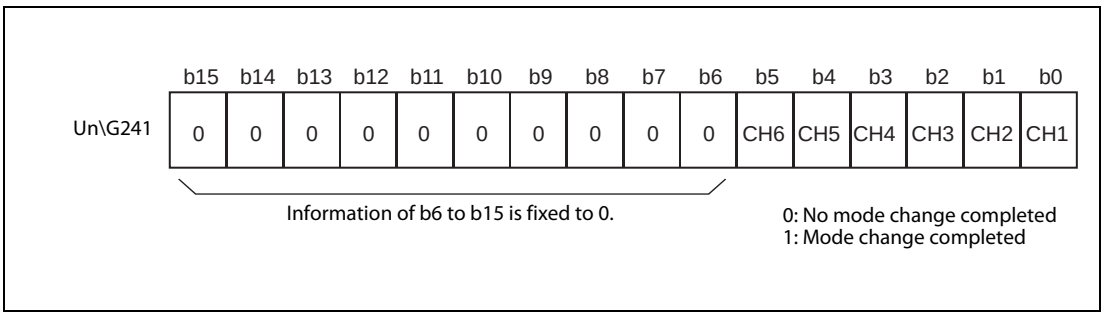


Fig. 4-11: *Assignment of the channel mode change complete flags*

CH□ Channel Mode Change Result (Un\G242, Un\G243...)

The result of the mode change is stored separately for each channel (Un\G242 to Un\G247).

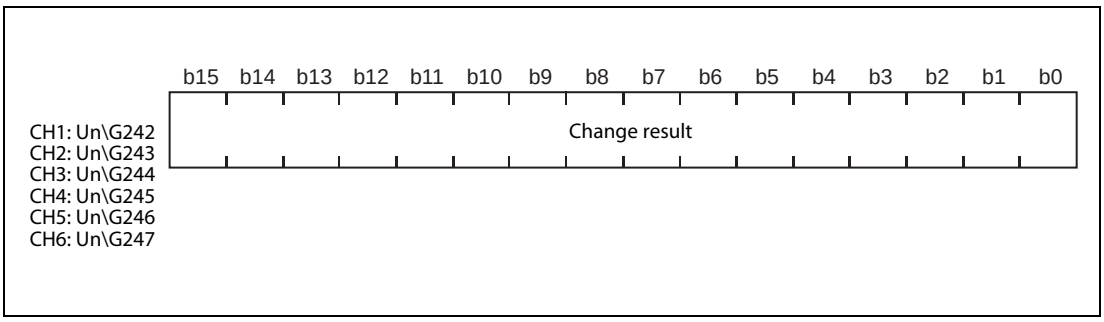


Fig. 4-12: *Assignment of bits for the channel mode settings*

Valid values for the CH□ Channel mode change result are shown in the following table.

Change result	Meaning	Description
0000_H	Success	—
0001_H	State Conflict	Mode setting is not supported.
0002_H	Wrong Cycle Time	The setting for the cycle time is invalid.
$E9FF_H$	Time out	—

Tab. 4-32: *Mode change results*

4.5.7 CH□ Current Mode (Un\G272, Un\G273...)

The actual mode of each channel is shown in the buffer memory address for CH□ current mode (Un\G272 to Un\G277). The format is the same as for "Mode setting" (refer to section 4.5.6).

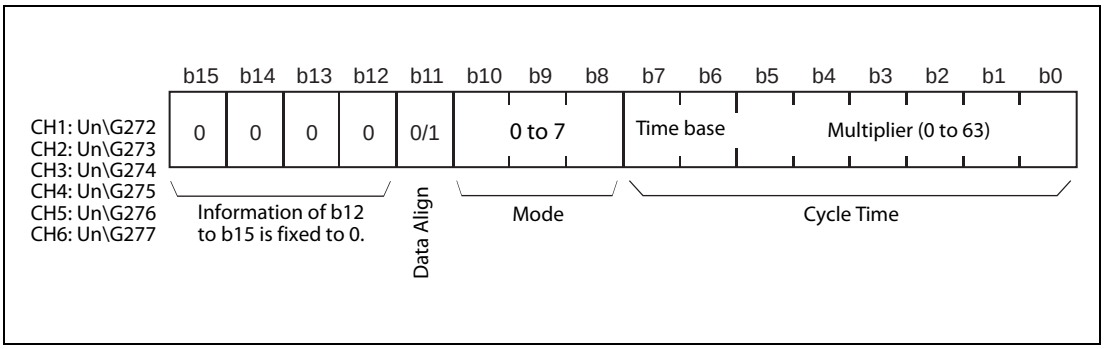


Fig. 4-13: *Assignment of the bits for the current channel mode*

4.5.8 Data Storage Setting (Un\G255)

The data storage function (section 4.3.10) can be enabled by setting the appropriate bits in the buffer memory address for data storage setting (Un\G255). In this buffer memory address, the user can select whether upload or download of data is enabled or disabled.

– Upload: Transfer of parameter data from the IO-Link device to the data storage area.

– Download: Transfer of parameter data from the data storage area to the IO-Link device.

As default, both the upload and the download is disabled for all channels.

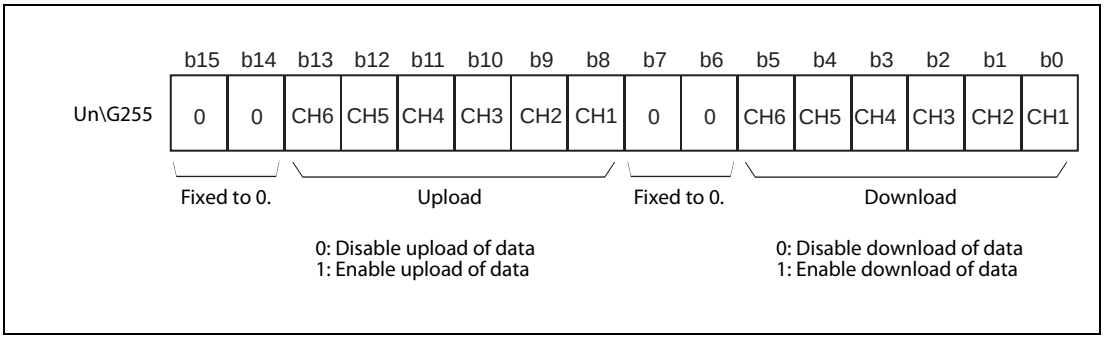


Fig. 4-14: *Assignment of the bits in buffer memory address Un\G255*

4.5.9 Current Data Storage Setting (Un\G279)

The current settings of the data storage function (section 4.3.10) can be checked in the buffer memory address Un\G279.

Whether to enable or disable the data storing function for each channel is set in Un\G255 (please refer to section 4.5.8).

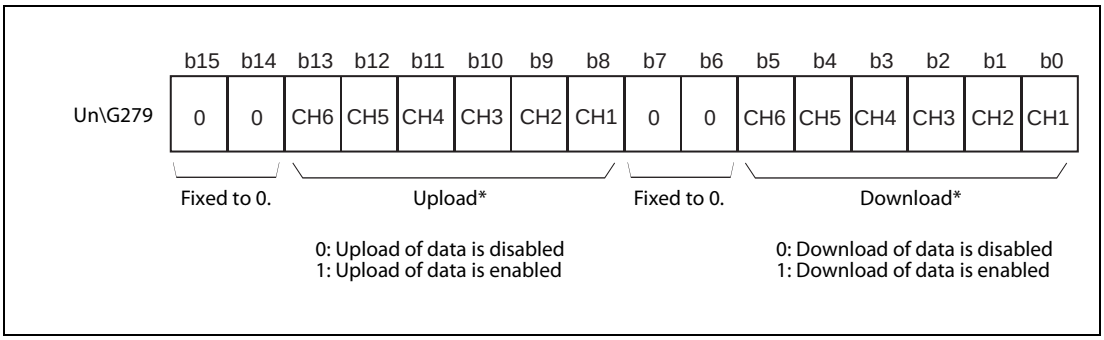


Fig. 4-15: *The bits in buffer memory address Un\G279 show whether upload or download is disabled or enabled.*

* Upload: Transfer of parameter data from the IO-Link device to the data storage.
Download: Transfer of parameter data from data storage to the IO-Link device.

4.5.10 Channel Error Flag (Un\G280), Channel Error Reset Flag (Un\G281)

When a channel error or a module error occurs, the corresponding bit in Un\G280 is set. In addition the error signal (XnF) will be switched ON and the LED of the corresponding channel lights up red. If the cause of the error disappears the red LED is switched OFF and the green LED indicates the current status of the channel.

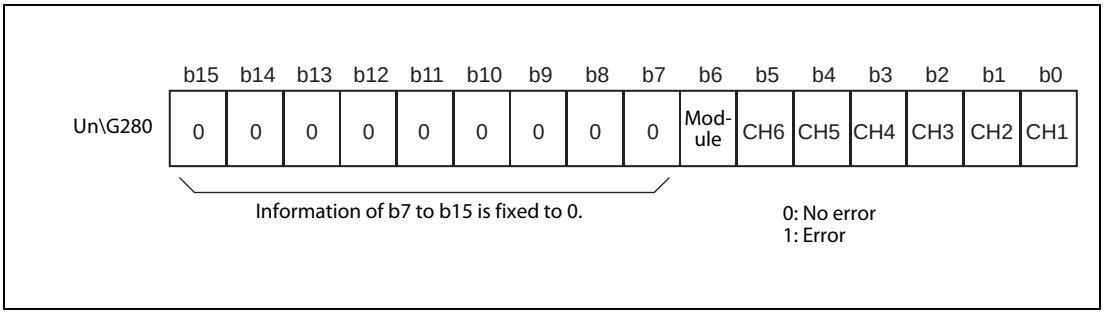


Fig. 4-16: *Assignment of the error flags*

The error can be confirmed/reset by setting the corresponding bit in Un\G281 (Error reset) after the cause for the error was resolved.

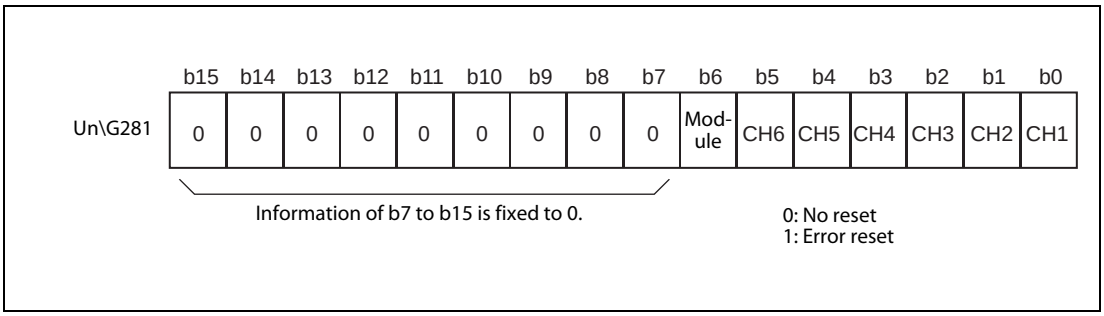


Fig. 4-17: *Assignment of the error reset flags*

When the error flags for all channels and the module are reset, the signal XnF will go OFF. The reset of the error will also cause the historical channel diagnostic flags to be cleared.

The timing of the signals is shown in the following figure.

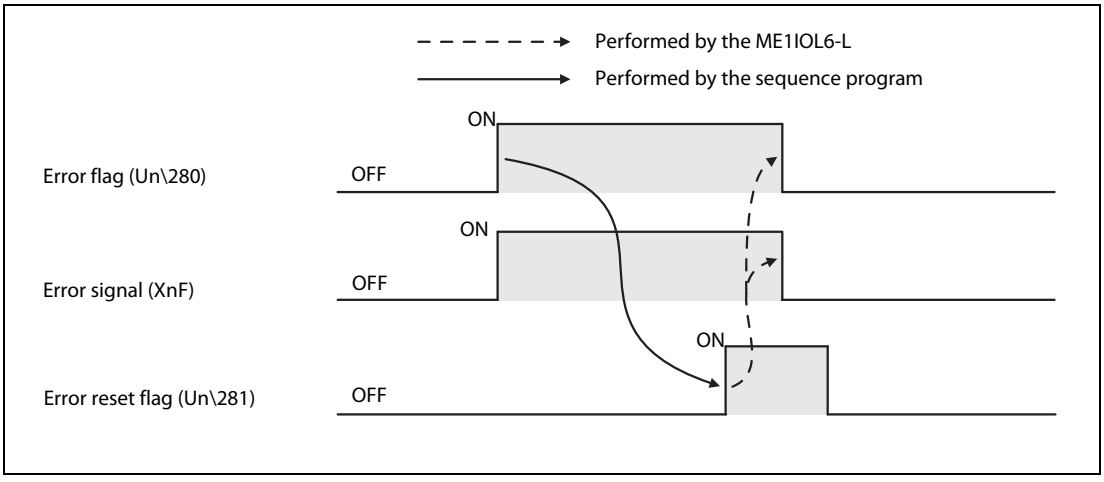


Fig. 4-18: *Timing of the error flags*

4.5.11 Module diagnostic information (Un\G282)

In case of a module error the cause of the error is shown in the module diagnostic information register (Un\G282).

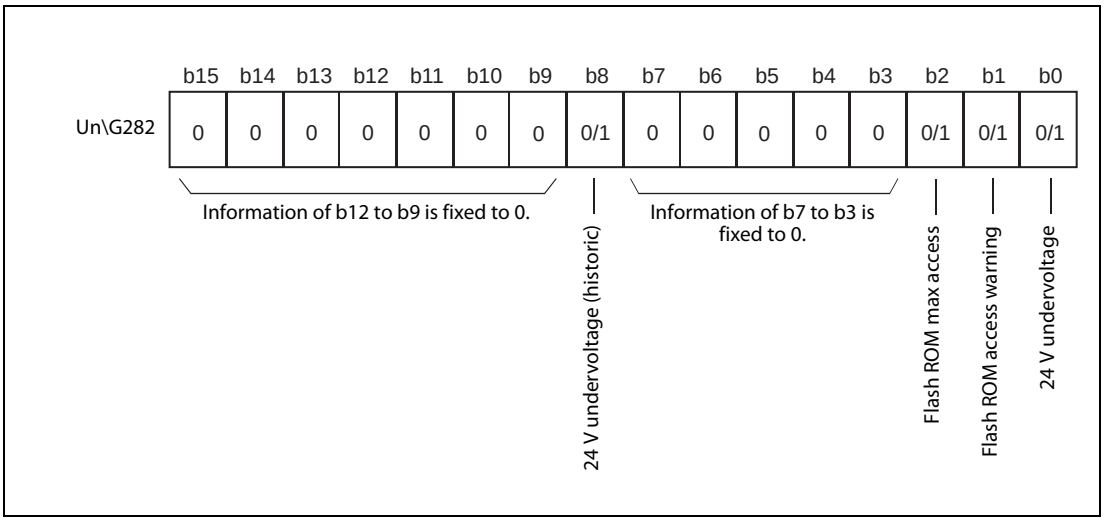


Fig. 4-19: *Assignment of the bits for the module diagnostic information*

The meaning of the bits b0 to b2 and b8 is as follows:

Bit	Meaning (when bit is set to "1")
b0	External 24 V DC undervoltage Delayed switch-on or no 24V after switch-on of the PLC are not shown as undervoltage fault.
b1	Flash ROM access warning Excessive amount of write accesses to flash ROM (more than 250 Writes in 24h). Flash ROM write access is terminated and after module or error reset the flash ROM access is working again.
b2	• The maximum number of flash ROM accesses has been reached, which is guaranteed by the flash ROM manufacturer. It is recommended to not use the data storage function any more or to replace the module. (This flag is not resetable.) • The flash ROM is not accessible and the data storage function is disabled.
b8	External 24 V DC undervoltage. The appearance of the 24 V fault is stored here until it has been confirmed by the user.

Tab. 4-33: *Module diagnostic information*

4.5.12 CH□ Diagnostic information (Un\G283, Un\G284...)

In case of an error at a channel the cause of the error is shown in the diagnostic information register of the corresponding channel (Un\G283 to Un\G288).

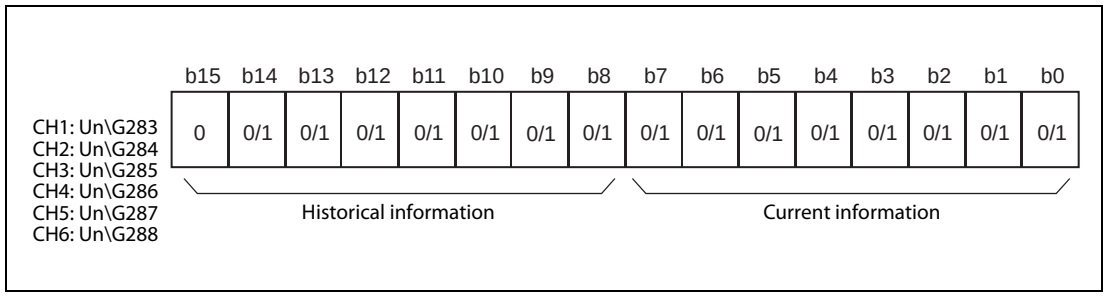


Fig. 4-20: *Assignment of the bits for the channel diagnostic information*

The CH□ diagnostic information is divided into flags for the current situation and flags, describing the historical appearance since the last error confirmation with the CH□ error reset flag (Un\G281). The meaning of the bits is as follows:

Bit	Meaning (when bit is set to "1")	Description
b0	L+ undervoltage	The voltage on the L+ line is too low.
b1	L+ overload	An overload has occurred on the L+ line.
b2	C/Q overload	An overload has occurred on the C/Q line.
b3	Overheat	The temperature is to high.
b4	Internal undervoltage fault	This fault can be caused by an undervoltage of the external 24 V DC power supply.
b5	Device error	• The IO-Link device validation is negative (refer to device validation). • The IO-Link device does not support the configured cycle time. The cycle time setting needs to be increased.
b6	Data storage error	An error in association with the data storage function has occurred.
b7	Device connected	• This bit is set to "1" when in IO-Link mode a device has been detected. • This bit is reset ("0") when a device is not present.
b8	L+ undervoltage	This is historical information. It is stored until the error has been confirmed by the user. For a more detailed description, please refer to the description of b0 to b6.
b9	L+ overload	
b10	C/Q overload	
b11	Overheat	
b12	Internal undervoltage fault	
b13	Device error	
b14	Data storage error	
b15	Fixed to 0.	—

Tab. 4-34: *Channel diagnostic information*

4.5.13 IO-Link event information (Un\G320 to Un\G370)

An IO-Link device can send event data to the master (ME1IOL6-L) to inform about certain states, problems, errors, etc. The ME1IOL6-L will store these events into the buffer memory.

Event flags (Un\G327)

When an event appears on one of the channels, the module will store the data of the event in the event information area of the channel (see below) and then set the corresponding bit in Un\327 to "1".

Additionally, the signal X(n+1)0 turns ON as long as there are any events pending. The signal will turn OFF when all events were confirmed.

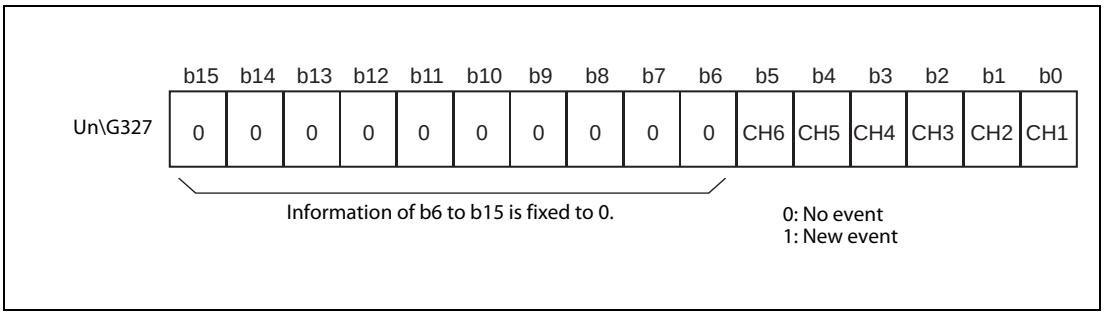


Fig. 4-21: *Assignment of the event flags*

Event reset flags (Un\G326)

The PLC has to acknowledge an event by setting the bit for the corresponding channel in Un\G326.

The ME1IOL6-L will ignore any further IO-Link events from that channel as long as the former one was not confirmed. This behaviour is necessary to keep the data in the event information area consistent.

When no more events are pending for any channel, resetting an event reset flag to "0" will cause the Event Signal (X(n+1)0) to turn OFF (refer to the figure on the following page).

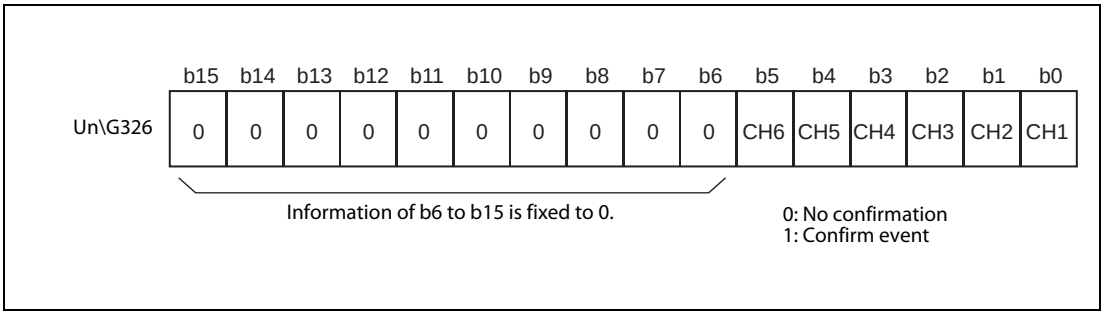


Fig. 4-22: *Assignment of the event reset flags*

NOTE

An event flag in Un\G327 will turn off after the corresponding event reset flag in Un\G326 has been set to "1".
An event reset flag should be set **after** processing the event information stored in the buffer memory because raising an event reset flag may cause the next event's data to be loaded into the buffer memory if there is any. Otherwise, the event data section will be reset to zero.

The indication and confirmation of events is shown in the following figure.

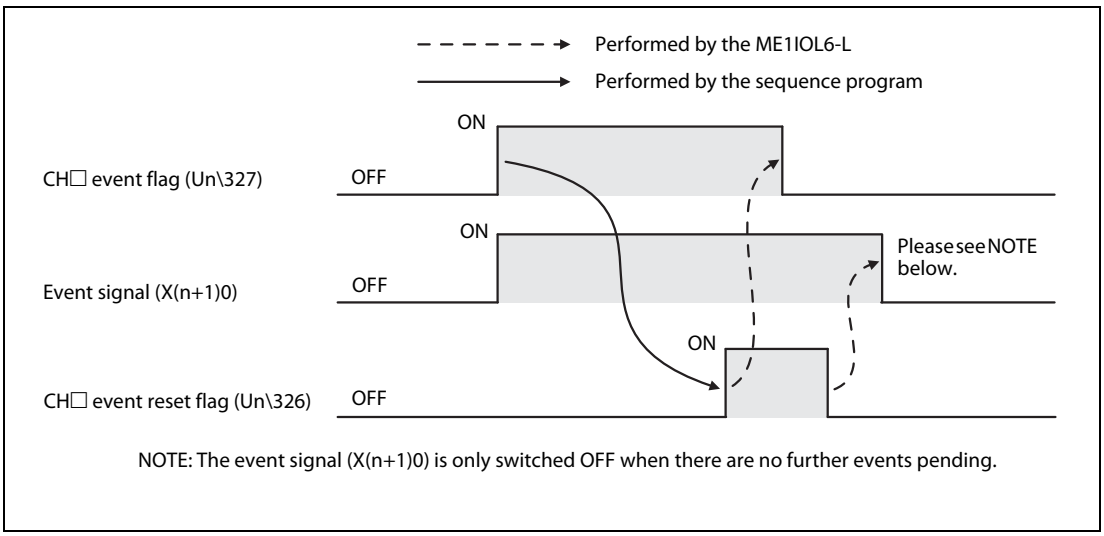


Fig. 4-23: *Timing of the event and event reset flags*

CH□ Event information area (Un\G328 to Un\G330, Un\G336 to Un\G338....)

The ME1IOL6-L stores events into the CH□ event information area. For each channel three words are reserved for event information, containing the detailed data of the latest event.

- Event ID

  Each event is assigned an unique ID (unique within the channel)

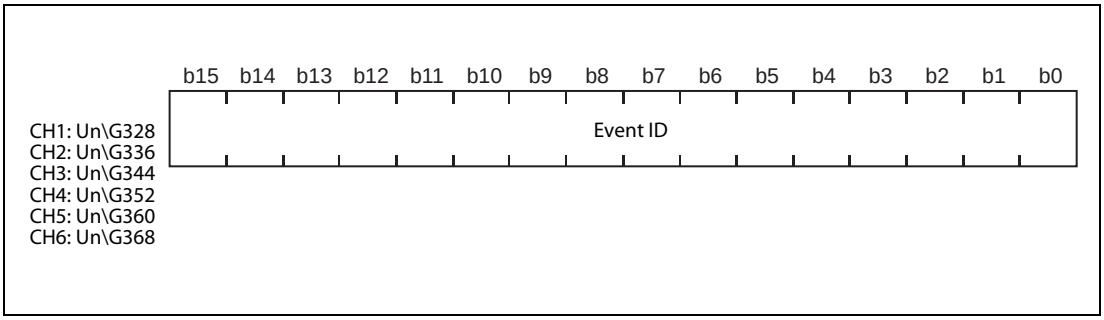


Fig. 4-24: *The event ID is unique within a channel.*

- Event Qualifier

  The contents of the event qualifier gives a detailed description of the event.

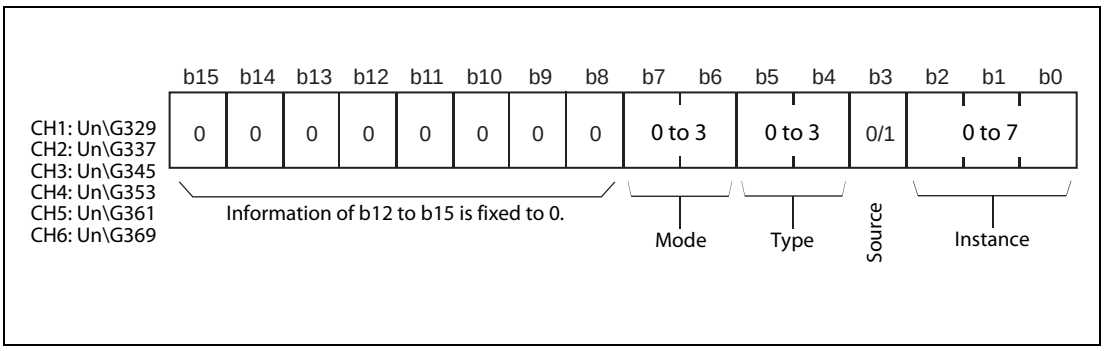


Fig. 4-25: *Assignment of the bits for the event qualifier*

– Instance

The meaning of the value for the instance is shown in the following table:

Instance				Description
Binary code			Value	
b2	b1	b0		
0	0	0	0	Unknown
0	0	1	1	PL (physical layer)
0	1	0	2	DL (data layer)
0	1	1	3	AL (application layer)
1	0	0	4	Application
1	0	1	5	Invalid
1	1	0	6	
1	1	1	7	

Tab. 4-35: *Event instances*

– Source

Bit 3 = "0": Device application (remote)

Bit 3 = "1": Master application (local)

– Type

Type			Description
Binary code		Value	
b5	b4		
0	0	0	Invalid
0	1	1	Notification
1	0	2	Warning
1	1	3	Error

Tab. 4-36: *Event types*

– Mode

Type			Description
Binary code		Value	
b7	b6		
0	0	0	Invalid
0	1	1	Event single shot
1	0	2	Event disappears (going)
1	1	3	Event appears (coming)

Tab. 4-37: *Event modes*

- Event code

  The event code is a 16 bit value defined by the IO-Link specification and the ME1IOL6-L just forwards it to the user as it is reported by the device. Depending on the source of the event, the meaning of the event code is either defined in the IO-Link specification or by the vendor of the device.

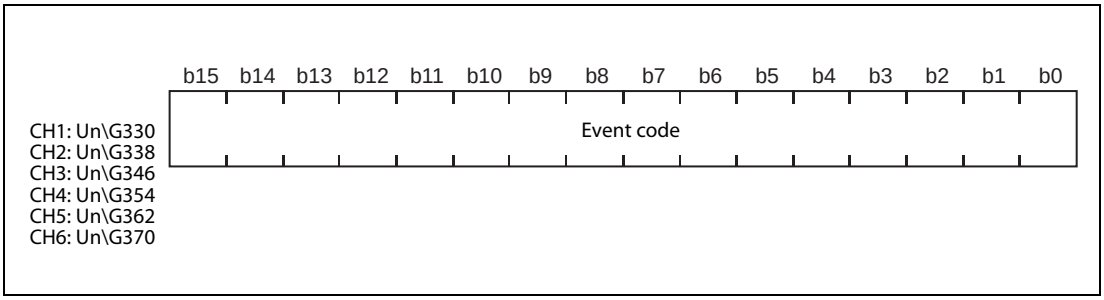


Fig. 4-26: *Buffer memory addresses for the event code.*

NOTE Please refer to the IO-Link specification for a detailed explanation of the event attributes.

CH□ Event Auto Confirmation Setting (Un\G320, Un\G321...)

The user can specify event types to be "ignored". These events will be confirmed automatically. The type of events to ignore can be set in the CH□ event auto confirmation setting.

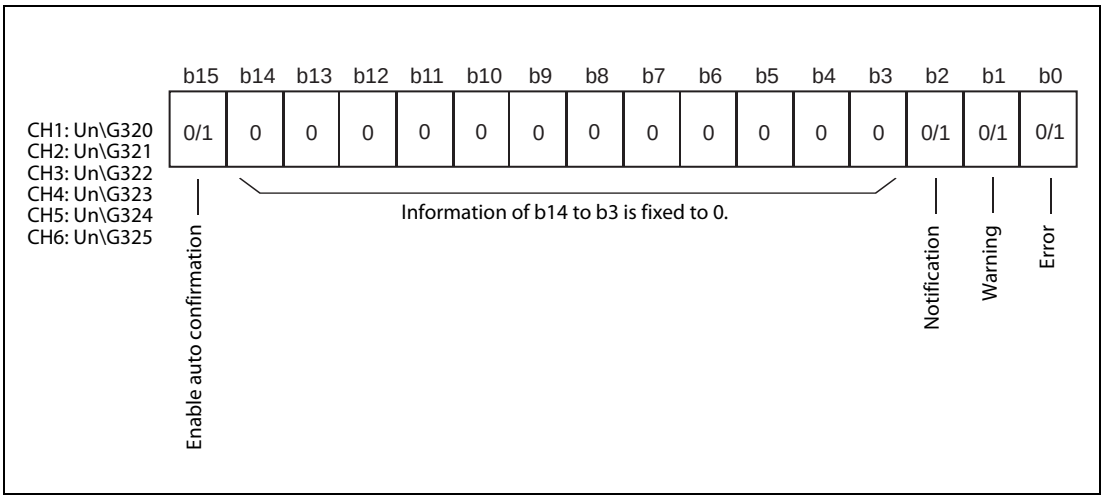


Fig. 4-27: *Assignment of the bits for the auto confirmation setting*

The meaning of the bits b0 to b2 and b8 is as follows:

Bit	Meaning	Description
b0	Auto confirmation of events of type Error	"0": No auto confirmation "1": Auto confirmation
b1	Auto confirmation of events of type Warning	
b2	Auto confirmation of events of type Error	
b15	Enable auto confirmation	"0": Auto confirmation is disabled for this channel. (The bits 0 to 2 have no affect.) "1": Auto confirmation is enabled for this channel

Tab. 4-38: *Four bits are used for the setting of auto confirmation*

NOTE The activation of the auto confirmation does only affect events issued AFTER the activation. It may be necessary to confirm an already pending event manually with the event reset flag (Un\G326).

4.5.14 CH□ Acyclic Communication Request (Un\G416 to Un\G1267)

In addition to the cyclic exchanged process data, a acyclic communication between the IO-Link master and an IO-Link device is also possible (see section 4.3.7).

In the buffer memory, 132 addresses are reserved for each channel storing the data required for an acyclic communication request:

- Command (1 word)
- Index (1 word)
- Subindex (1 word)
- Data size (1 word)
- Data (128 words)

CH□ Command (Un\G416, Un\G560...)

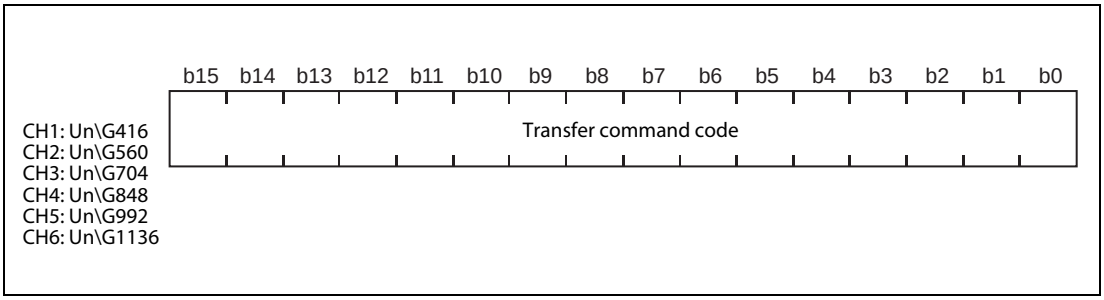


Fig. 4-28: *Buffer memory addresses for the acyclic communication request command code.*

The valid command codes are shown in the following table.

Command (hexadecimal)	Meaning	
0100H	Read request	
0101H	Write request	
0102H	Command abort request	
0200H	Data storage	Data read request
0201H		Data write request
0202H		Configuration Request
0301H	Device validation (write)	

Tab. 4-39:
Communication request commands

NOTE

Other request codes than described above will return an result code of FFFFH in the acyclic communication answer data (refer to section 4.5.17).

CH□ Index (Un\G417, Un\G561...)

The index is used to address the parameter to access. Valid index values are 0 to 32767.

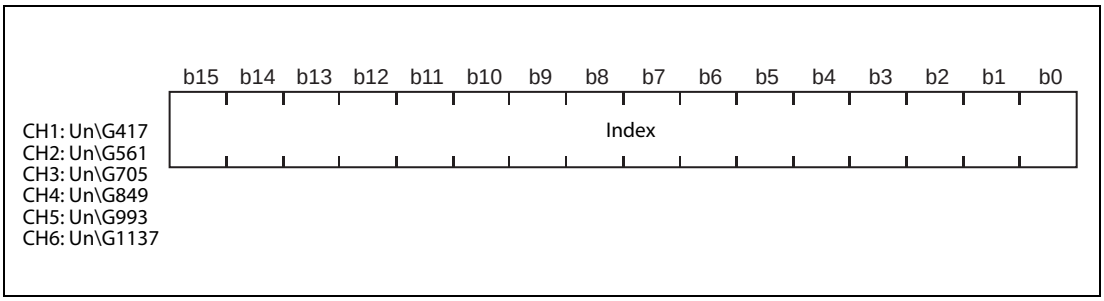


Fig. 4-29: *Buffer memory addresses for the acyclic communication request index*

CH□ Sub index (Un\G418, Un\G562...)

The sub index defines the offset within the parameter. Valid sub index values are 0 to 231.

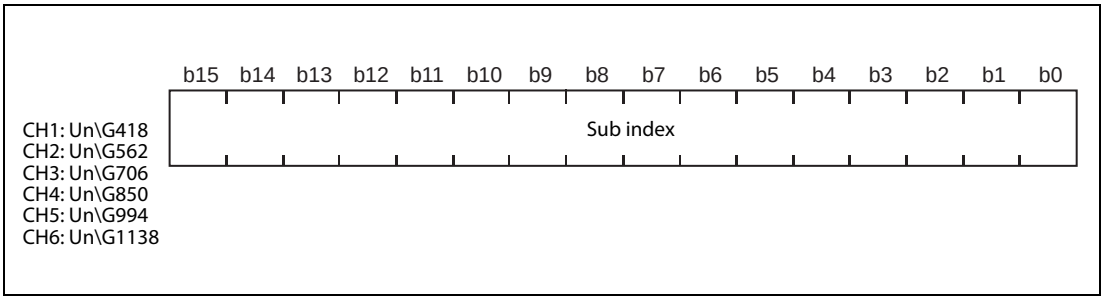


Fig. 4-30: *Buffer memory addresses for the sub index of the acyclic communication request*

CH□ Data size (Un\G419, Un\G563...)

In case of a write request, the data size defines the amount of bytes to be transferred. Valid values for the data size are 0 to 254 [bytes].

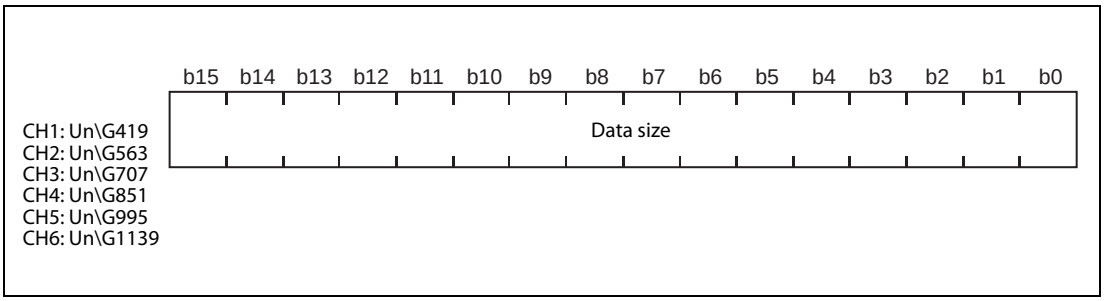


Fig. 4-31: *Buffer memory addresses for the acyclic communication request data size*

CH□ Data (Un\G420 to Un\G547, Un\G564 to Un\G691...)

For the data transmitted with a write request, 128 words of buffer memory are reserved for each channel.

Address	Channel	Description
Un\G420	CH1	Data (128 words)
to		
Un\G547		
Un\G564	CH2	Data (128 words)
to		
Un\G691		
Un\G708	CH3	Data (128 words)
to		
Un\G835		
Un\G852	CH4	Data (128 words)
to		
Un\G979		
Un\G996	CH5	Data (128 words)
to		
Un\G1123		
Un\G1140	CH6	Data (128 words)
to		
Un\G1267		

Tab. 4-40:
Buffer memory addresses for the channel data (acyclic communication request)

4.5.15 Acyclic Communication Request Flags (Un\G1280)

To issue a request for acyclic communication (section 4.3.7) the appropriate bit in the buffer memory address Un\G1280 must be set. Afterwards the request stored in the acyclic communication request data area for the corresponding channel (section 4.5.14) is transmitted to the IO-Link device.

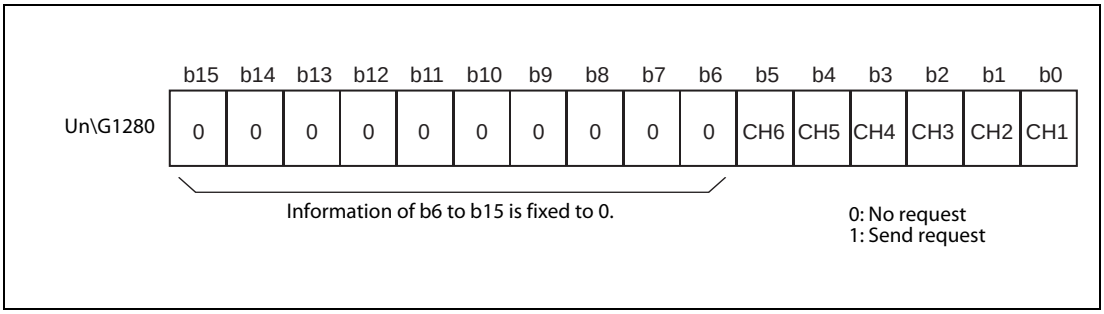


Fig. 4-32: *Assignment of the bits in buffer memory address Un\G1280*

4.5.16 Acyclic Communication Response Flags (Un\G1281)

The contents of Un\G1281 shows the state of an acyclic communication request. The bits in the high-byte show that the transaction is accepted/started and the low-byte shows the completion of the channels transaction.

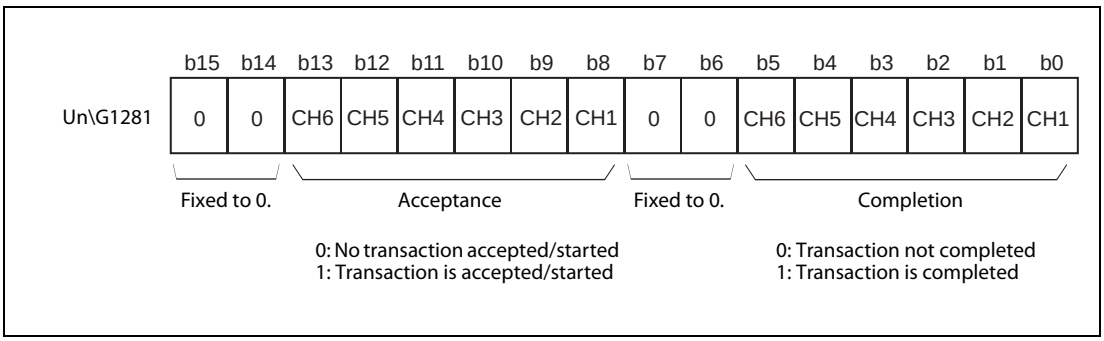


Fig. 4-33: *Assignment of the bits in buffer memory address Un\G1281*

4.5.17 CH□ Acyclic Communication Answer (Un\G1296 to Un\G2148)

In addition to the cyclic exchanged process data, acyclic communication between the IO-Link master and an IO-Link device is also possible (section 4.3.7).

When the IO-Link master sends a request for acyclic communication to an IO-link device (refer to section 4.5.14), the device answers and the data received by the master is stored in the buffer memory. For each channel the following area is reserved for the response data:

- Command (1 word)
- Index (1 word)
- Subindex (1 word)
- Result (1 word)
- Data size (1 word)
- Data (128 words)

CH□ Command (Un\G1296, Un\G1440...)

The transfer command code sent in the answer is the same as in the request area (section 4.5.14).

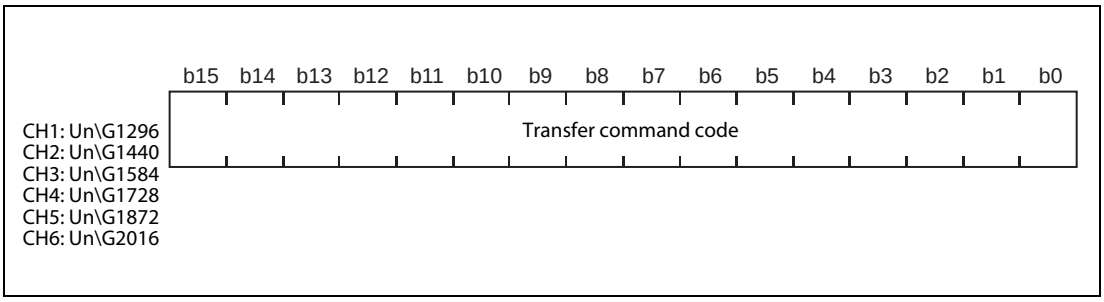


Fig. 4-34: *Buffer memory addresses for the transfer command code in the answer*

CH□ Index (Un\G1297, Un\G1441...)

The index sent in the answer is the same as in the request area (refer to section 4.5.14).

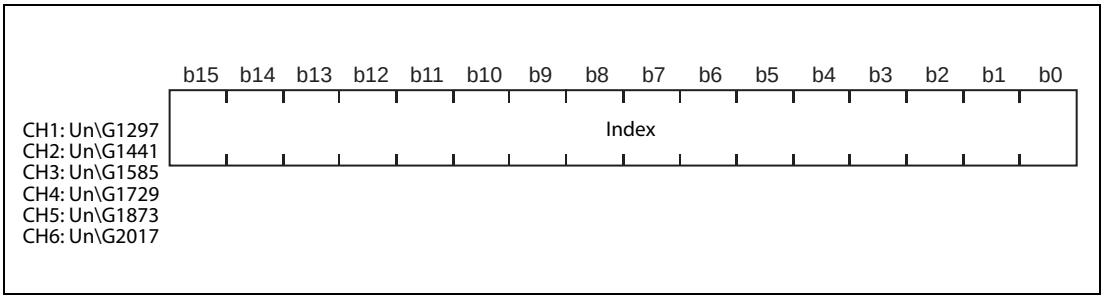


Fig. 4-35: *Buffer memory addresses for the index in the acyclic communication answer*

CH□ Sub index (Un\G1298, Un\G1442...)

The index sent in the answer is the same as in the request area (refer to section 4.5.14).

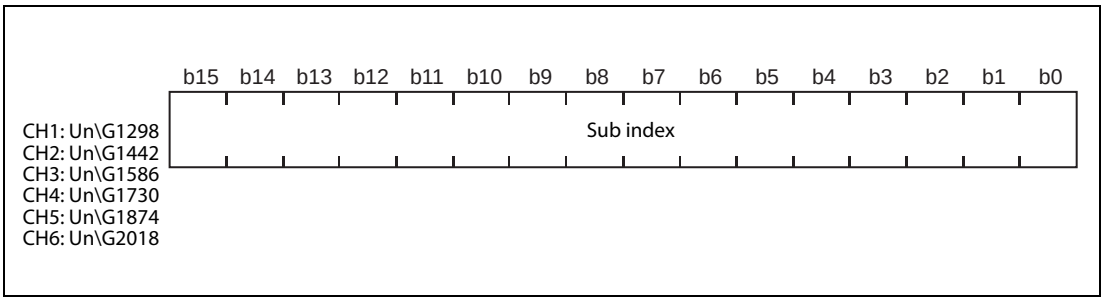


Fig. 4-36: *Buffer memory addresses for the sub index in the acyclic communication answer*

CH□ Result (Un\G1299, Un\G1443...)

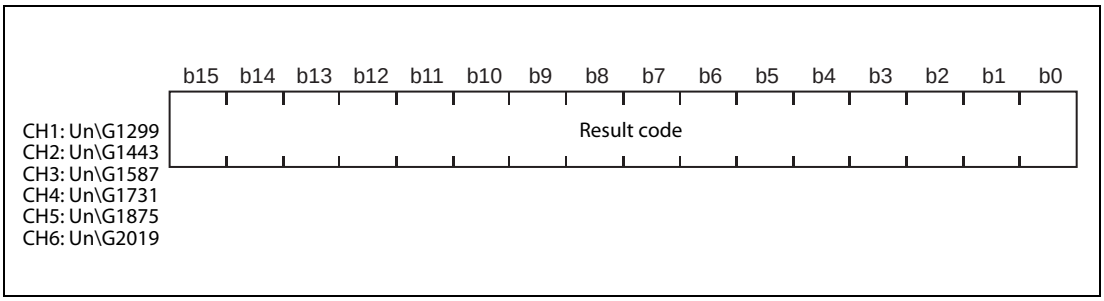


Fig. 4-37: *Buffer memory addresses for the result of the acyclic communication request.*

The result of the acyclic communication request is stored as hexadecimal code.

Result (hexadecimal)	Meaning
0000_H	The operation was successful.
1100_H	The operation was aborted due to time-out.
$E0FF_H$	The operation could not be performed (channel not in IO-Link mode, invalid index etc.)
$FFFF_H$	The requested command code is not supported.

Tab. 4-41: *Acyclic communication request results*

NOTE

Any other result code indicates that the request itself has been executed but there were errors on IO-Link level. For the meaning of those result codes please refer to the IO-Link specification.

CH□ Data size (Un\G1300, Un\G1444...)

In case of a read request, the data size defines the amount of bytes sent in the answer. Valid values for the data size are 0 to 254 [bytes].

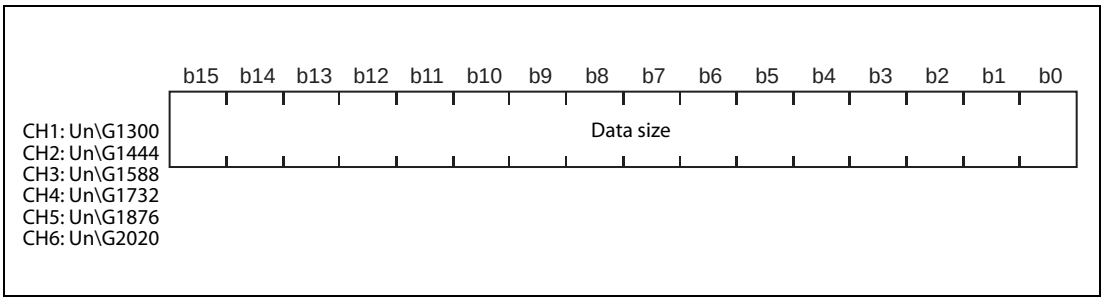


Fig. 4-38: *Buffer memory addresses for the size of the received data*

CH□ Data (Un\G1301 to Un\G1428, Un\G1445 to Un\G1572...)

For the data transmitted with an answer, 128 words of buffer memory are reserved for each channel.

Address	Channel	Description
Un\G1301	CH1	Data (128 words)
to		
Un\G1428		
Un\G1445	CH2	Data (128 words)
to		
Un\G1572		
Un\G1589	CH3	Data (128 words)
to		
Un\G1716		
Un\G1733	CH4	Data (128 words)
to		
Un\G1860		
Un\G1877	CH5	Data (128 words)
to		
Un\G2004		
Un\G2021	CH6	Data (128 words)
to		
Un\G2148		

Tab. 4-42:
Buffer memory addresses for the channel data (acyclic communication answer)

4.5.18 Direct Parameter Page 1 (DPP1) Read Access

The direct parameter page 1 (DPP1) of an IO-Link device, containing device information and data specifications, can be directly read by the master module. The DPP1 has a size of 16 bytes.

CH□ Direct parameter page 1 (DPP1) read request flags (Un\G2158)

Each channel has a direct parameter page 1 read area in the buffer memory. This area can be updated by setting the appropriate bits in the buffer memory address for direct parameter page 1 (DPP1) read request (Un\G2158).

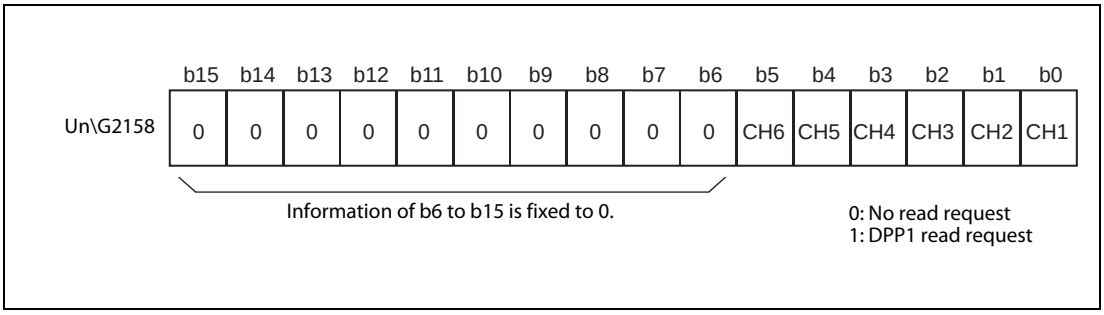


Fig. 4-39: *Assignment of the bits in buffer memory address Un\G2158*

CH□ Direct parameter page 1 (DPP1) read response flags (Un\G2159)

The direct parameter page 1 (DPP1) read response flags in Un\G2159 indicate that data is available in the corresponding buffer memory area.

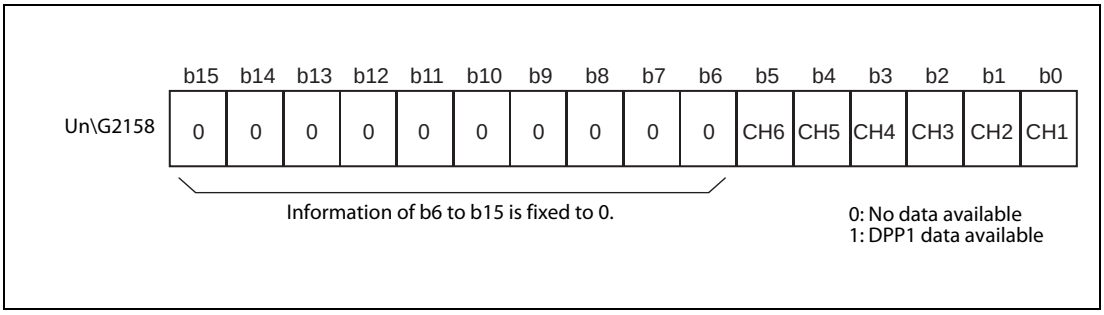


Fig. 4-40: *Assignment of the bits in buffer memory address Un\G2159*

5 Setup and Procedures before Operation

5.1 Handling Precautions

- Do not drop the module or subject it to heavy impact.
- Do not remove the PCB of the module from its case. Doing so may cause the module to fail.
- Prevent foreign matter such as dust or wire chips from entering the module. Such foreign matter can cause a fire, failure, or malfunction.
- Before handling the module, touch a grounded metal object to discharge the static electricity from the human body.

  Failure to do so may cause the module to fail or malfunction.
- Tighten the screws such as module fixing screws within the following ranges. Loose screws may cause short circuits, failures, or malfunctions.

Screw location	Tightening torque range
Terminal block screws (M3 screws)	0.42 to 0.58 Nm
Terminal block mounting screws (M3.5 screws)	0.66 to 0.89 Nm

Tab. 5-1: *Tightening torques*

5.2 Getting started

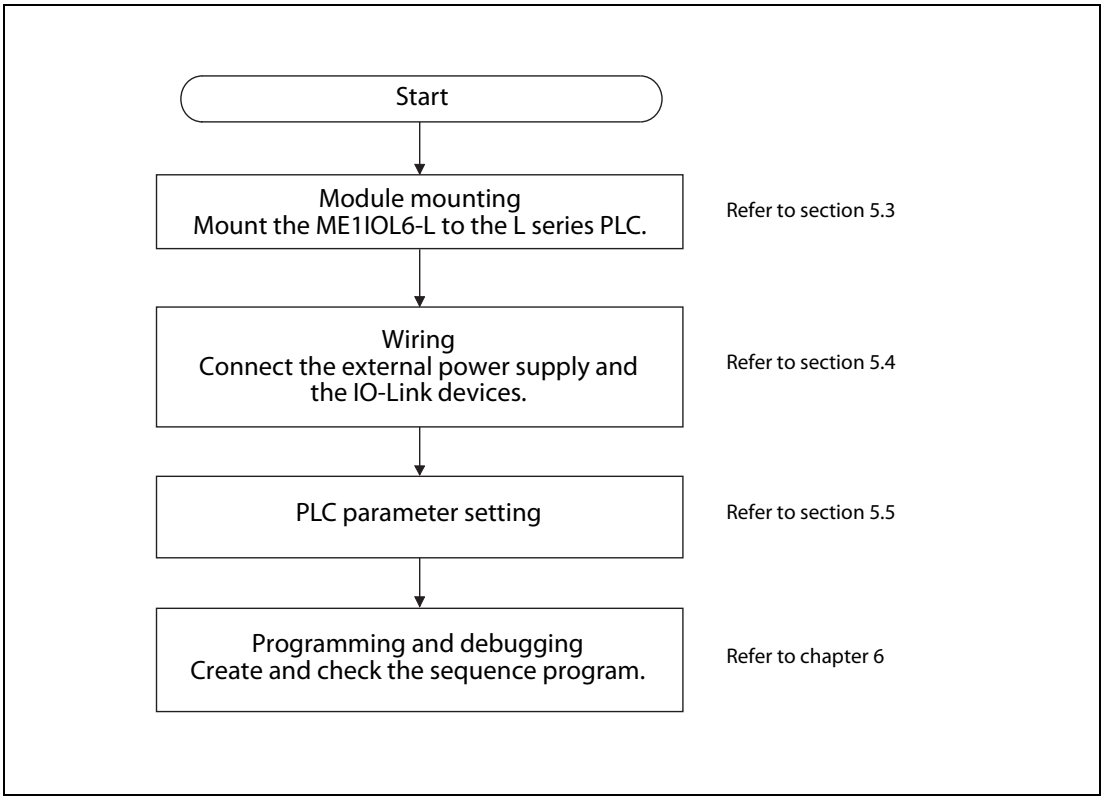


Fig. 5-1: *Function chart for the setup of an IO-Link master module ME1IOL6-L*

5.3 Installation Environment and Installation Position

For installation environment and installation position, please refer to the User's Manual for the CPU modules of the MELSEC-L series (Hardware design, Maintenance and Inspection).

5.3.1 Safety Precautions

Design Precautions

WARNING:

- ***Configure safety circuits external to the programmable controller to ensure that the entire system operates safely even when a fault occurs in the external power supply or the programmable controller. Failure to do so may result in an accident due to an incorrect output or malfunction.***
  - ***– Emergency stop circuits, protection circuits, and protective interlock circuits for conflicting operations (such as forward/reverse rotations or upper/lower limit positioning) must be configured external to the programmable controller.***
  - ***– When the programmable controller detects an abnormal condition, it stops the operation and all outputs are:***
    - ***Turned off if the overcurrent or overvoltage protection of the power supply module is activated.***
    - ***Held or turned off according to the parameter setting if the self-diagnostic function of the CPU module detects an error such as a watchdog timer error.***

    Also, all outputs may be turned on if an error occurs in a part, such as an I/O control part, where the CPU module cannot detect any error. To ensure safety operation in such a case, provide a safety mechanism or a fail-safe circuit external to the programmable controller. For a fail-safe circuit example, refer to "GENERAL SAFETY REQUIREMENTS" in the manual "Safety Guidelines" included in the CPU module or head module.
  - ***– Outputs may remain on or off due to a failure of a component such as a relay and transistor in an output circuit. Configure an external circuit for monitoring output signals that could cause a serious accident.***
- ***In an output circuit, when a load current exceeding the rated current or an overcurrent caused by a load short-circuit flows for a long time, it may cause smoke and fire. To prevent this, configure an external safety circuit, such as a fuse.***
- ***Configure a circuit so that the programmable controller is turned on first and then the external power supply. If the external power supply is turned on first, an accident may occur due to an incorrect output or malfunction.***
- ***When changing data of a running programmable controller from a peripheral device connected to the CPU module to the running programmable controller, configure an interlock circuit in the program to ensure that the entire system will always operate safely.***

  For other controls to a running programmable controller (such as program modification or operating status change), read relevant manuals carefully and ensure the safety before the operation.

  Especially, in the case of a control from an external device to a remote programmable controller, immediate action cannot be taken for a problem on the programmable controller due to a communication failure. To prevent this, configure an interlock circuit in the program, and determine corrective actions to be taken between the external device and CPU module in case of a communication failure.

Installation Precautions

DANGER:

- ***Cut off all phases of the power source externally before starting the installation or wiring work.***

WARNING:

- ***Use the programmable controller in an environment that meets "GENERAL SPECIFICATIONS" in the manual "Safety Guidelines" included in the CPU module or head module. Failure to do so may result in electric shock, fire, malfunction, or damage to or deterioration of the product.***
- ***To interconnect modules, engage the respective connectors and securely lock the module joint levers. Incorrect interconnection may cause malfunction, failure, or drop of the module.***
- ***Do not directly touch any conductive parts and electronic components of the module. Doing so can cause malfunction or failure of the module.***

5.4 Wiring

5.4.1 Wiring precautions

DANGER:

- ***Cut off all phases of the power source externally before starting the installation or wiring work.***
- ***After installation and wiring, attach the included terminal cover to the module before turning it on for operation. Failure to do so may result in electric shock.***

WARNING:

- ***Check the rated voltage and terminal layout before wiring to the module, and connect the cables correctly. Connecting a power supply with a different voltage rating or incorrect wiring may cause a fire or failure.***
- ***Connectors for external devices must be crimped or pressed with the tool specified by the manufacturer, or must be correctly soldered. Incomplete connections may cause short circuit, fire, or malfunction.***
- ***Tighten the terminal block screw within the specified torque range. Undertightening can cause short circuit, fire, or malfunction. Overtightening can damage the screw and/or module, resulting in drop, short circuit, fire, or malfunction.***
- ***When disconnecting the cable from the module, do not pull the cable by the cable part. For the cable connected to the terminal block, loosen the terminal screw. Pulling the cable connected to the module may result in malfunction or damage to the module or cable.***
- ***Prevent foreign matter such as dust or wire chips from entering the module. Such foreign matter can cause a fire, failure, or malfunction.***

Please observe the following precautions for external wiring:

- Do not lay control lines or communication cables close to the main circuit, high-voltage power lines, or load lines. Otherwise effects of noise or surge induction are likely to take place. Keep a safe distance of more than 100 mm from the above when wiring.
- The FG terminal of the ME1IOL6-L must be connected to the ground certainly.
- Observe the following items for wiring the terminal block. Ignorance of these items may cause electric shock, short circuit, disconnection, or damage of the product:
  - Use solderless terminals for the connection. Twist the end of stranded wires and make sure there are no loose wires.
  - Solderless terminals with insulating sleeves cannot be used for the terminal block. Covering the cable-connection portion of the solderless terminal with a marked tube or an insulation tube is recommended.
  - Do not solder-plate the electric wire ends.
  - Connect only electric wires of regular size.
  - Tightening of terminal block screws should follow the torque described on page 5.1.
  - Fix the electric wires so that the terminal block and connected parts of electric wires are not directly stressed.

5.4.2 External wiring

For the wiring method, and how to remove or install a terminal block, please refer to the User's Manual for the CPU modules of the MELSEC-L series (Hardware design, Maintenance and Inspection).

Although the ME1IOL6-L is a IO-Link master module, it is possible to mix conventional devices (in SIO mode) with IO-Link devices.

To each channel of the ME1IOL6-L one device can be connected in a point-to-point configuration. Multidrop network connection (more than one device to one channel) is not possible.

Applicable cables

For the connection of IO-Link devices, standardized 3-conductor cables or, in the control cabinet, individual leads are used. No shield is required.

The maximum extension for each individual connection is 20 m. The resistance and the capacity of the cable should not exceed 6 Ω resp. 3 nF.

The recommended minimum gauge values must be observed. For 20 m cable length the minimum cross-section is 0.34 mm^2.

External power supply

For operation of the ME1IOL6-L, an external power supply of 24 V DC (+20%, -15%, which gives a voltage range of 20.4 to 28.8 V DC), is required.

NOTE

In order to keep the specified IO-Link output voltage levels (L+ line) the external supply voltage must be higher than 22 V DC.

Connection of the external wiring

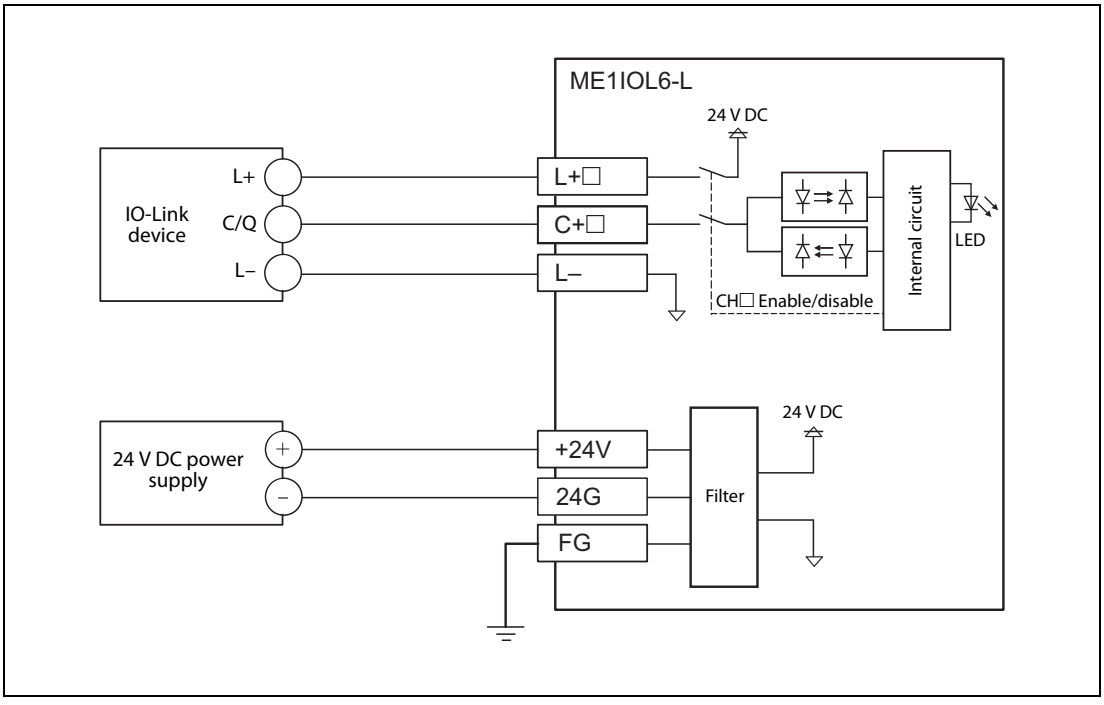


Fig. 5-2: *External wiring of the ME1IOL6-L*

Noise filter (external power supply line filter)

A noise filter is a component which has an effect on conducted noise.

It is not required to attach the noise filter to the external power supply line, however attaching it can suppress more noise.

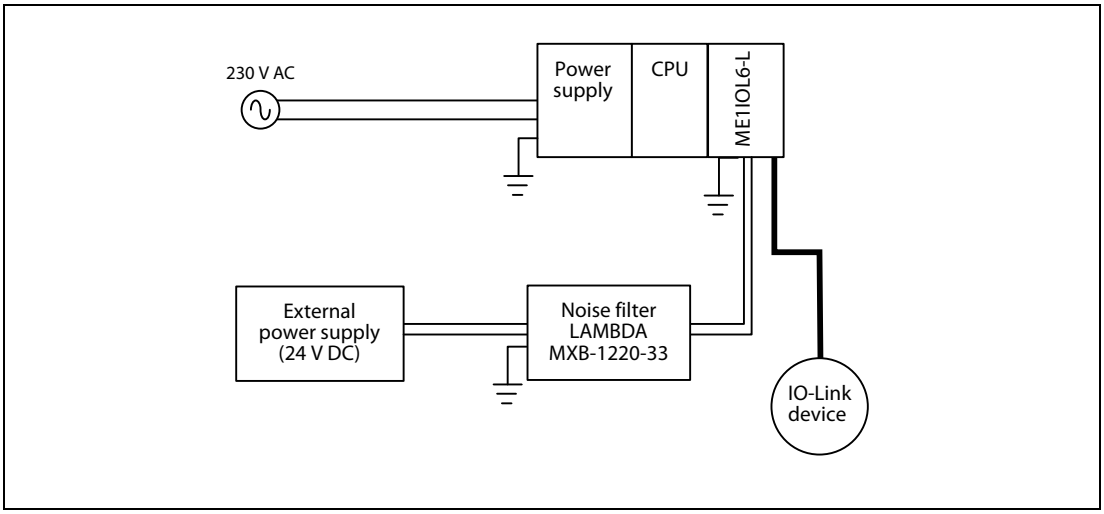


Fig. 5-3: *Noise filter connection*

The precautions required when installing a noise filter are described below.

- Ground the noise filter grounding terminal to the control cabinet with the shortest wire possible.
- Do not bundle the wires on the external power supply side and ME1IOL6-L side of the noise filter. When bundled, the external power supply side noise will be induced into the ME1IOL6-L side wires from which the noise was filtered (refer to the below figure.).

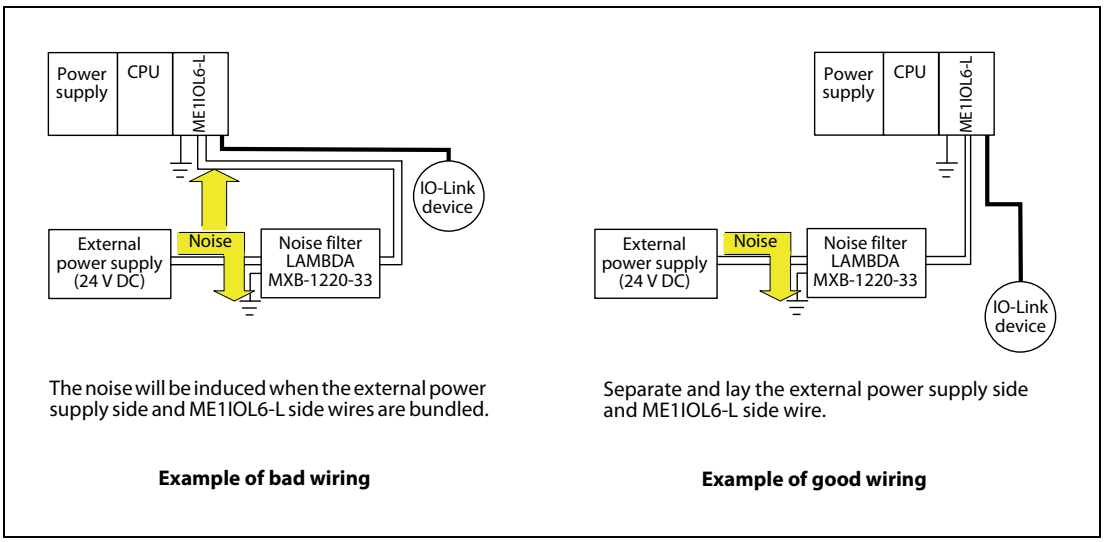


Fig. 5-4: *Precautions on noise filter*

The following noise filter is recommended.

Noise filter model		**MXB-1220-33**
Maker		LAMBDA
Rated output	Voltage	250 V AC, 250 V DC
	Current	20 A

Tab. 5-2:
Recommended noise filter

5.5 PLC Parameter Setting

In the PLC parameters the I/O assignment for the ME1IOL6-L and the HOLD/CLEAR function are set.

5.5.1 I/O assignment

Start GX Works2 and open up the project with the ME1IOL6-L. After the selection of ***Parameter*** in the Project Navigator Window, double click on ***PLC parameter***.

The L parameter setting window will appear. Click on the ***I/O Assignment*** tab.

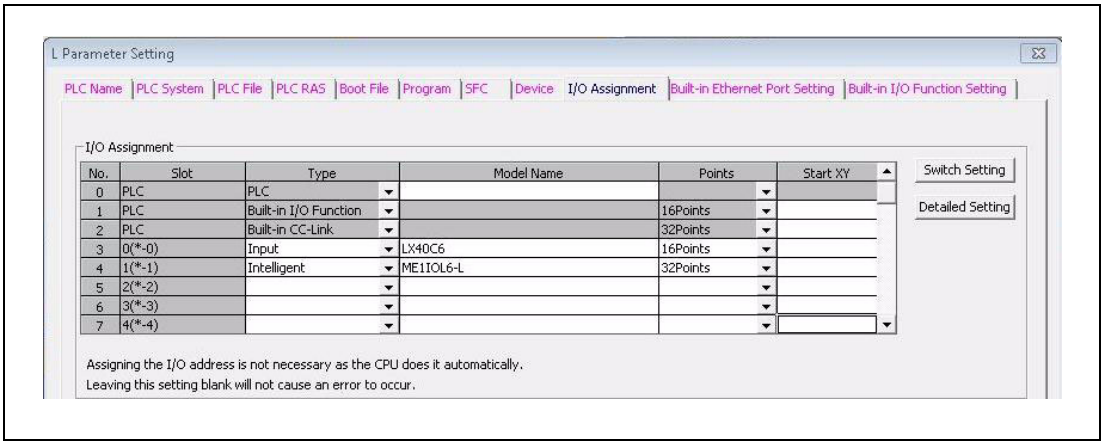


Fig. 5-5: *I/O assignment setting screen*

Set the following for the slot in which the ME1IOL6-L is mounted:

Type: Select "Intelligent"

Model name: ME1IOL6-L (Entering of the module model name is optional. The entry is used for documentation only and has no effect on the function of the module.)

Points: Select 32 points.

Start XY: Start I/O number for the ME1IOL6-L. (Assigning of the I/O address is not necessary as the address is automatically assigned by the PLC CPU.)

5.5.2 Intelligent function module switch settings

The HOLD/CLEAR setting for each channel of the ME1IOL6-L is selected by a "switch" in the PLC parameters. There are no switches at the module itself.

The intelligent function module switches are set using 16 bit data (4 hexadecimal digits).

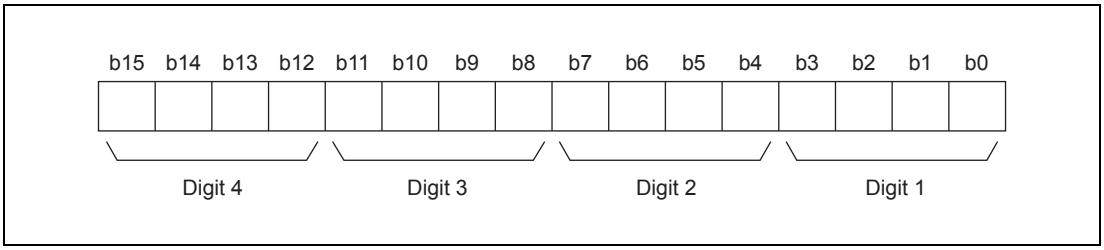


Fig. 5-6: *Bit assignment for one switch*

In the I/O assignment setting screen (section 5.5.1) click on ***Switch Setting*** to display the screen shown below, then set the switches as required. The switches can easily be set if values are entered in hexadecimal. Change the entry format to hexadecimal and then enter the values.

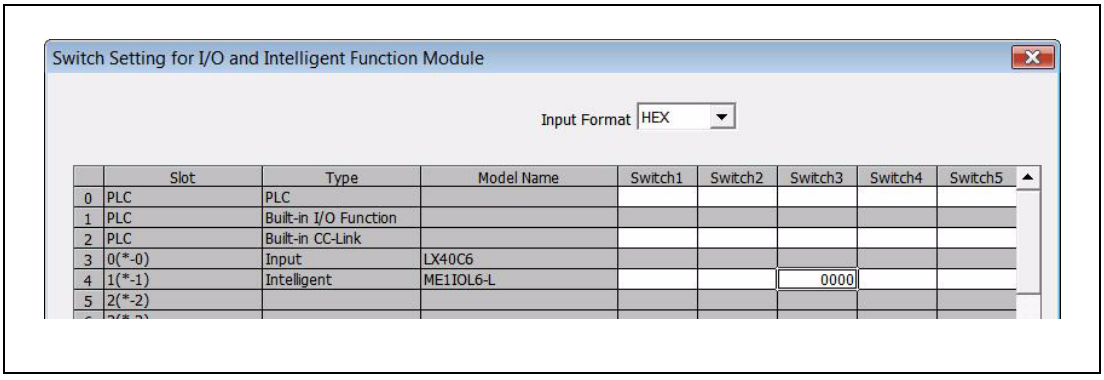


Fig. 5-7: *Switch setting for intelligent function modules*

When the intelligent function module switches are not set, the default value for switches 1 to 5 is 0000H.

Switch 3 is used to define the behaviour of the

- output signals Yn1 to Yn6 (SIO output mode) and the
- output data valid signals Y(n+1)1 to Y(n+6)1 (IO-Link mode).

Switch	Setting item	
Switch 1	Reserved	Fixed to 0H
Switch 2	Reserved	
Switch 3	HOLD/CLEAR function setting (CH1 to CH6) b15 ~ b6 b5 b4 b3 b2 b1 b0 0 ~ 0 CH6 CH5 CH4 CH3 CH2 CH1	HOLD/CLEAR function setting 0: CLEAR the output 1: HOLD the output
Switch 4	Reserved	Fixed to 0H
Switch 5	Reserved	

Tab. 5-3: *Switch settings for the ME1IOL6-L*

5.6 Setting of the IO-Link Devices

For setting the parameters of the IO-Link devices, a commercially available FDT/DTM* can be used.

* FDT stands for **F**ield **D**evice **T**ool and DTM stands for **D**evice **T**ype **M**anager. FDT/DTM is a communication technique for the manufacturer-independent configuration of field devices.

For connection to an IO-Link device, CPU port connection (USB, Ethernet) as well as Ethernet networks can be used.

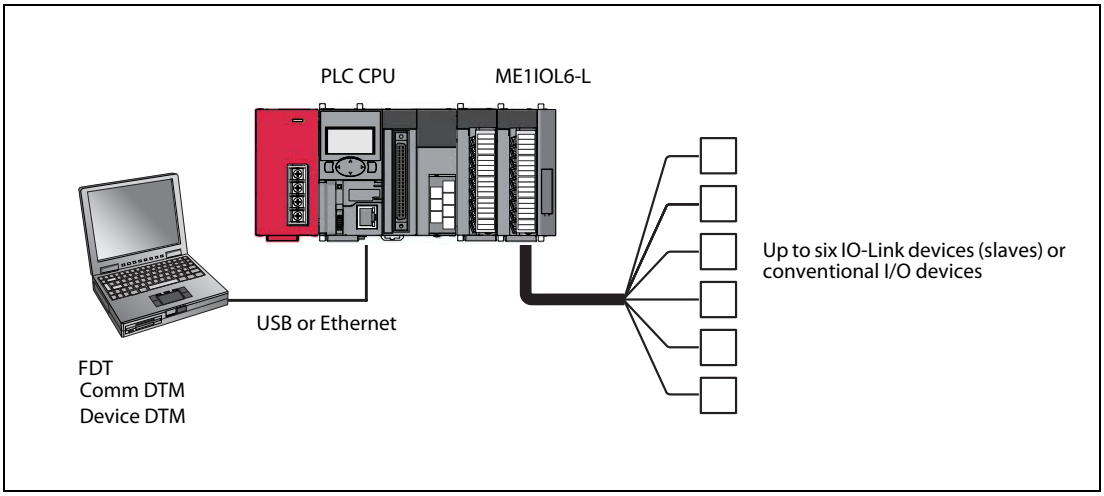


Fig. 5-8: *System configuration for the connection to the PLC CPU*

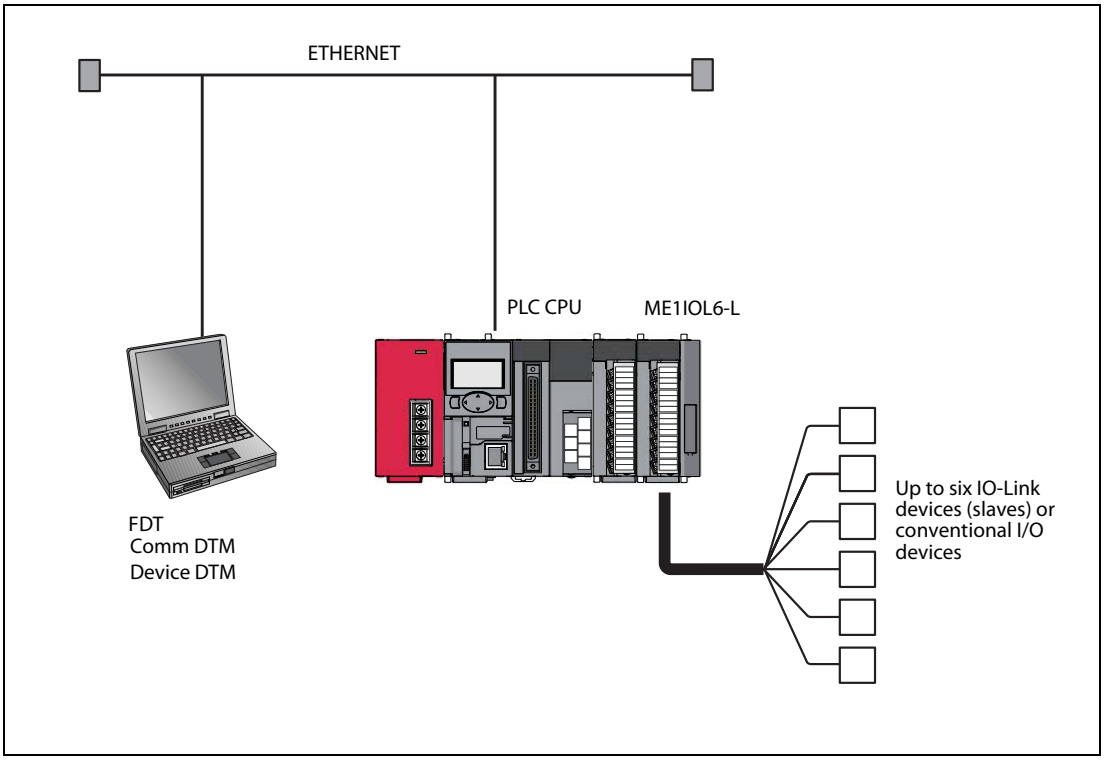


Fig. 5-9: *System configuration for an Ethernet connection*

- IODD (IO-Link Device Description) for each IO-Link device

  Please ask the manufacturer of the IO-Link device.

6 Programming

This chapter describes the programming of the IO-Link master module ME1IOL6-L.

NOTE When applying any of the program examples introduced in this chapter to the actual system, verify the applicability and confirm that no problems will occur in the system control.

6.1 Programming Procedure

Create a program that will execute the data exchange with IO-Link devices in the following procedure.

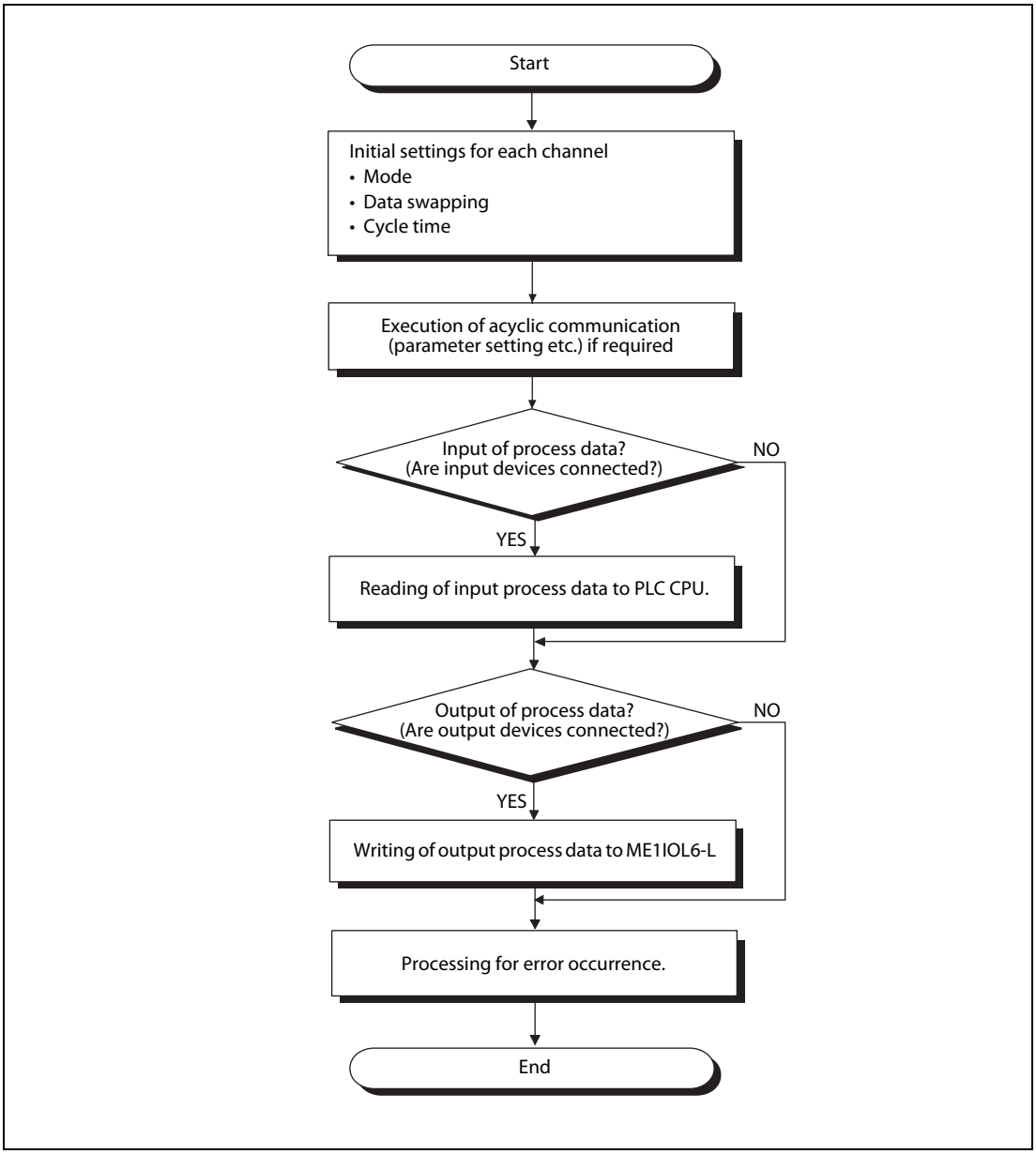


Fig. 6-1: *Programming procedure for the ME1IOL6-L*

6.2 Example 1: Input of Process Data

System configuration

The following figure shows the system configuration used for this example. For the sake of simplicity, only one IO-Link device which exchanges process data with the master module is connected to the ME1IOL6-L.

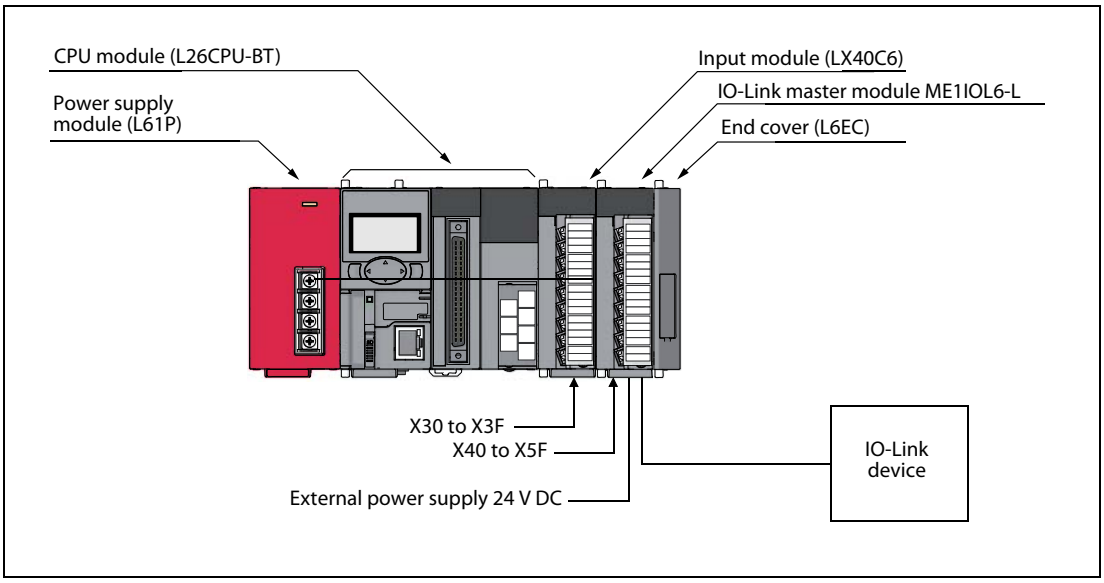


Fig. 6-2: *In this and the following examples the ME1IOL6-L is mounted to the CPU module together with an input module.*

Channel	HOLD/CLEAR function setting
CH1	CLEAR
CH4 to CH6	—

Tab. 6-1: *Conditions for the intelligent function module switch setting*

Program conditions

- CH1 is used in IO-Link mode for the input of process data (refer to sections 4.5.2 and 4.5.6.).
- In the event of a module error, a message shall be displayed on the display unit of the PLC CPU. The error shall be reset after removal of the cause.
- A warning lamp is switched ON if the device connected to channel 1 is malfunctioning. The CH1 error shall be reset after removal of the cause.

6.2.1 Before creating a program

Perform the following steps before creating a program.

Wiring of external devices

Mount the ME1IOL6-L to the MELSEC-L series PLC and connect the external power supply and the IO-Link device. For details, refer to section 5.4.2.

Switch setting in the PLC parameters

Based on the setting conditions given on the previous page, make the switch settings for the intelligent function module in the PLC parameters. The HOLD/CLEAR setting is set to CLEAR by default. Please note, that the switches are not stored in the module, so checking and setting of the switches is always required even if the module was used before in an other application.

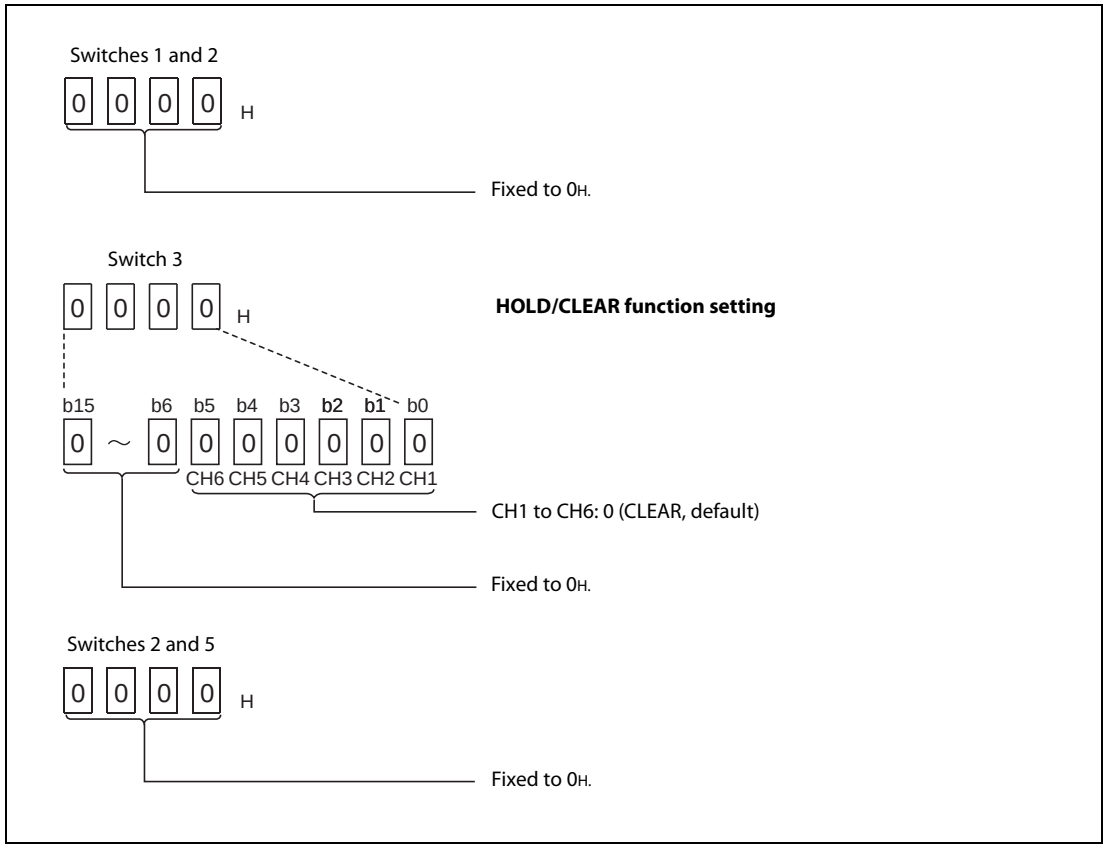
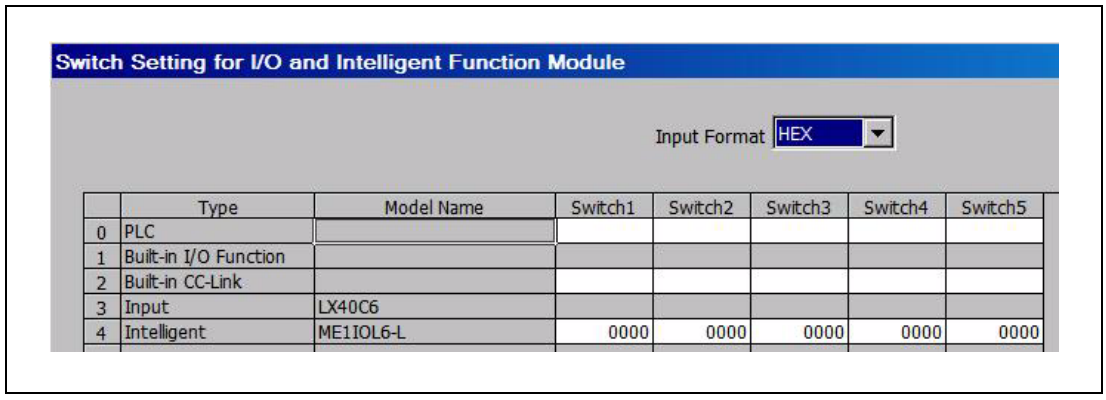


Fig. 6-3: *Setting of the switches 1 to 5 for this example*

On the **Parameter setting** screen of GX Works2, select the ***I/O assignment*** tab, click ***Switch setting***, and make settings of the switches 1 to 5 as on the screen shown below (for details about the setting, refer to section 5.5.2).



	Type	Model Name	Switch1	Switch2	Switch3	Switch4	Switch5
0	PLC						
1	Built-in I/O Function						
2	Built-in CC-Link						
3	Input	LX40C6					
4	Intelligent	ME1IOL6-L	0000	0000	0000	0000	0000

Fig. 6-4: *Switch setting for this example*

6.2.2 Program

For full documentation of all the instructions used with examples please refer to the Programming Manual for the MELSEC System Q and the MELSEC-L series.

List of used devices

Device		Function	Remark
Inputs	X30	Error reset signal	LX40C6 (X30 to X3F)
	X40	Module ready	ME1IOL6-L (X40 to X5F)
	X47	External power (24 V DC) ready	
	X4F	Error	
	X51	CH1: input data invalid	
Outputs	Y7	Warning lamp: IO-Link error	L26CPU-BT (Y0 to Y7)
Internal relays	M10	Initialization of CH1 completed without fault	The mode for CH1 has been changed without fault.
	M11	Error during initialization of CH1	An error has occurred during mode changing for CH1.
Register	D100 to D115	CH1: Input process data in IO-Link mode	The contents of D100 to D115 corresponds to the contents of Un\G0 to Un\G15.
	D120	CH1: Diagnostic information	The contents of D120 corresponds to the contents of Un\G283.

Tab. 6-2: *List of used devices*

Program parts

- Initial settings

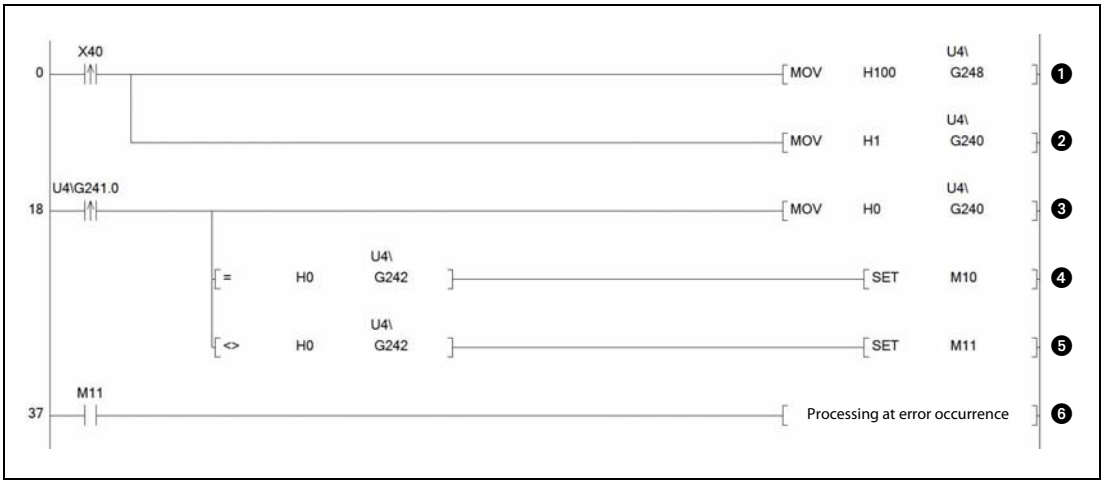


Fig. 6-5: *The channel mode setting is performed once when X40 (Module ready) turns on.*

Number	Description
❶	CH1 is set to: IO-Link mode, data swapping, fastest possible cycle time
❷	The channel mode change flag of CH1 is set.
❸	After the channel mode change complete flag of CH1 is set, the channel mode change flag of CH1 is reset.
❹	When the result of the channel mode change for CH1 is "0" the initialization has been completed without error. In this case M10 is set.
❺	M11 (Error occurrence) is set, when the result of the channel mode change for CH1 is not "0".
❻	These instructions are only executed when an error has occurred during mode changing.

Tab. 6-3: *Description of the program for the initial settings*

- Reading of input process data

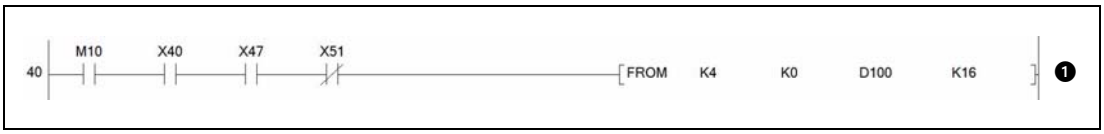


Fig. 6-6: *The input data is stored in the registers D100 to D115.*

Number	Description
❶	The input process data of CH1 is moved from the buffer memory of the ME1IOL6-L to the PLC CPU when • the changing of the channel mode has been completed without an error (M10) • the IO-Link master module is ready (X40) • the external power supply (24 V DC) is ON (X47) • and the input data on CH1 is valid (X51).

Tab. 6-4: *Description of the program shown above*

- Processing for a module error

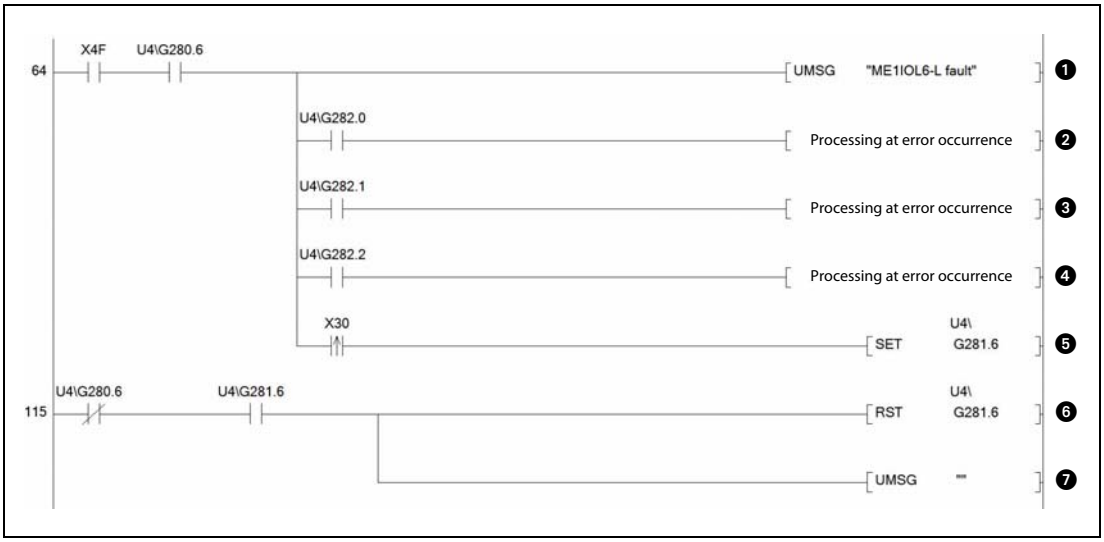


Fig. 6-7: *Program part for module error processing*

Number	Description	
❶	When a module error is detected (Un\G280.6), the message "ME1IOL6-L fault" is displayed on the display unit of the CPU module.	
❷	Processing at error occurrence	External 24 V DC undervoltage
❸		Flash ROM access warning
❹		Maximum number of flash ROM accesses
❺	When X30 (Error reset signal) is switched ON while the module error flag is ON, the error reset flag for a module error is set.	
❻	When there is no module error indicated, the error reset flag is reset.	
❼	Without a module error, the user message on the display unit is cleared.	

Tab. 6-5: *Description of the program shown above*

- Processing for a channel error

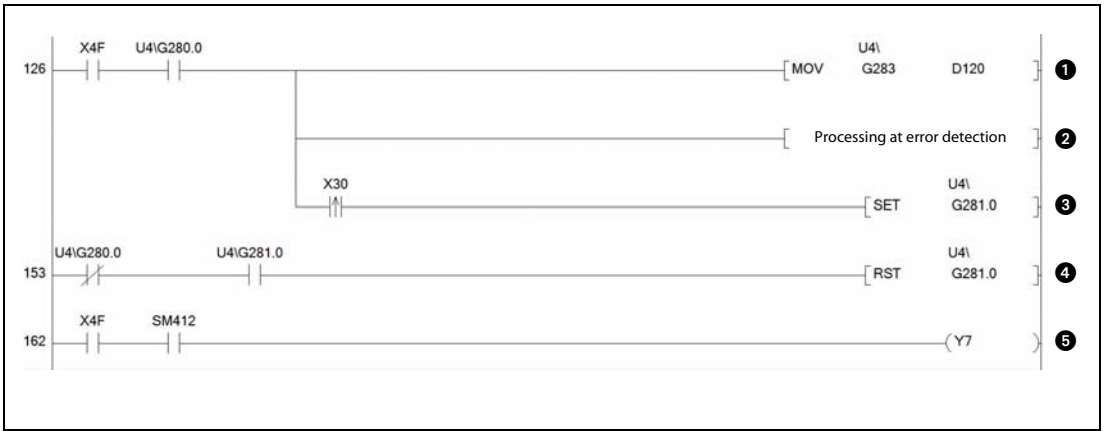


Fig. 6-8: *Sequence program for error handling*

Number	Description
❶	When the error detection flag for CH1 is ON (Un\G280.0), the diagnostic information for CH1 is moved to the register D120.
❷	Processing at error detection for CH1.
❸	When X30 (Error reset signal) is switched ON while the CH1 error flag is ON, the error reset flag for CH1 is set.
❹	When there is no error indicated for CH1, the error reset flag is reset.
❺	An module error or an error at channel 1 is indicated by a flashing lamp. SM412 is a 1 second clock signal.

Tab. 6-6: *Description of the program shown above*

6.3 Example 2: Output of Process Data

System configuration

In this example, data is output to an IO-Link device connected to channel 1 of a ME1IOL6-L. The same system configuration as for example 1 is used (refer to section 6.2).

Program conditions

- CH1 is used in IO-Link mode for the output of process data (refer to section 4.5.3.).
- In the event of a module error, a message shall be displayed on the display unit of the PLC CPU. The error shall be reset after removal of the cause.
- A warning lamp is switched ON if the device connected to channel 1 is malfunctioning. The CH1 error shall be reset after removal of the cause.

6.3.1 Before creating a program

Before creating the program, perform the steps described in section 6.2.1.

6.3.2 Program

For full documentation of all the instructions used with examples please refer to the Programming Manual for the MELSEC System Q and the MELSEC-L series.

List of used devices

Device		Function	Remark
Inputs	X30	Error reset signal	LX40C6 (X30 to X3F)
	X40	Module ready	ME1IOL6-L (X40 to X5F)
	X47	External power (24 V DC) ready	
	X4F	Error	
Outputs	Y7	Warning lamp: IO-Link error	L26CPU-BT (Y0 to Y7)
	Y51	CH1: Output data valid	ME1IOL6-L (Y40 to Y5F)
Internal relays	M10	Initialization of CH1 completed without fault	The mode for CH1 has been changed without fault.
	M11	Error during initialization of CH1	An error has occurred during mode changing for CH1.
Register	D120	CH1: Diagnostic information	The contents of D120 corresponds to the contents of Un\G283.
	D130 to D145	CH1: Output process data in IO-Link mode	The contents of D130 to D145 is transferred to the buffer memory addresses Un\G112 to Un\G127.

Tab. 6-7: *List of used devices*

Program parts

- Initial settings

  The initial settings are the same as performed for example 1 (please refer to section 6.2.2).

- Writing of output process data

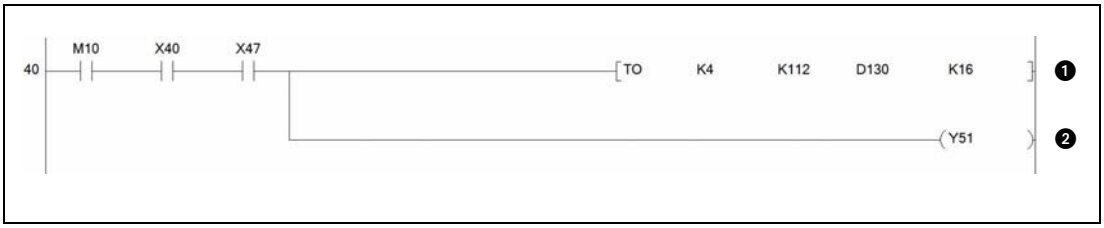


Fig. 6-9: *The output data is stored in the registers D130 to D145.*

Number	Description
❶	The output process data for CH1 is moved from the PLC CPU to the buffer memory of the ME1IOL6-L when • the changing of the channel mode has been completed without an error (M10) • the IO-Link master module is ready (X40) • and the external power supply (24 V DC) is ON (X47).
❷	The output signal "CH1 output data valid" is turned ON when the conditions mentioned above are satisfied. Every change of the contents of the registers D130 to D145 is reflected by the data sent to the IO-Link device.

Tab. 6-8: *Description of the program shown above*

- Processing for a module error

  The processing for an error of the ME1IOL6-L is the same as performed for example 1 (please refer to section 6.2.2).

- Processing for a channel error

  The processing for an error at channel 1 is the same as performed for example 1 (please refer to section 6.2.2).

6.4 Example 3: Acyclic Communication (Reading)

System configuration

In this example, data is read from an IO-Link device connected to channel 1 of a ME1IOL6-L using acyclic communication. The same system configuration as for example 1 is used (refer to section 6.2).

Program conditions

- CH1 is used in IO-Link mode (refer to section 4.5.3.).
- The header information for acyclic communication is stored in registers. This allows for an easy change of command, index and subindex.
- The read data is transferred from the buffer memory to registers for further processing.

6.4.1 Before creating a program

Before creating the program, perform the steps described in section 6.2.1.

6.4.2 Program

For full documentation of all the instructions used with examples please refer to the Programming Manual for the MELSEC System Q and the MELSEC-L series.

List of used devices

Device		Function		Remark
Inputs	X31	Acyclic communication start signal		LX40C6 (X30 to X3F)
	X40	Module ready		ME1IOL6-L (X40 to X5F)
Internal relay	M10	Initialization of CH1 completed without fault		The mode for CH1 has been changed without fault.
Register	D150	Acyclic communication request	Command	The header information required for the request is stored in these registers by instructions elsewhere in the program.
	D151		Index	
	D152		Sub-index	
	D154	Acyclic communication answer	Data size	Unit: Byte
	D155	Data size (Number of received data)		Unit: Word
	D156	Remainder of division operation		Used for calculation of the data size.
	D1000 to D1127	Read data from the IO-Link device at CH1		The buffer memory addresses Un\G1301 to Un\G1428 are reflected in D1000 to D1127. Un\G1301 -> D1000 Un\G1302 -> D1001 .... Un\G1428 -> D1127

Tab. 6-9: *List of used devices for acyclic communication (reading)*

Program parts

- Initial settings

  The initial settings are the same as performed for example 1 (please refer to section 6.2.2).

- Reading of data using acyclic communication

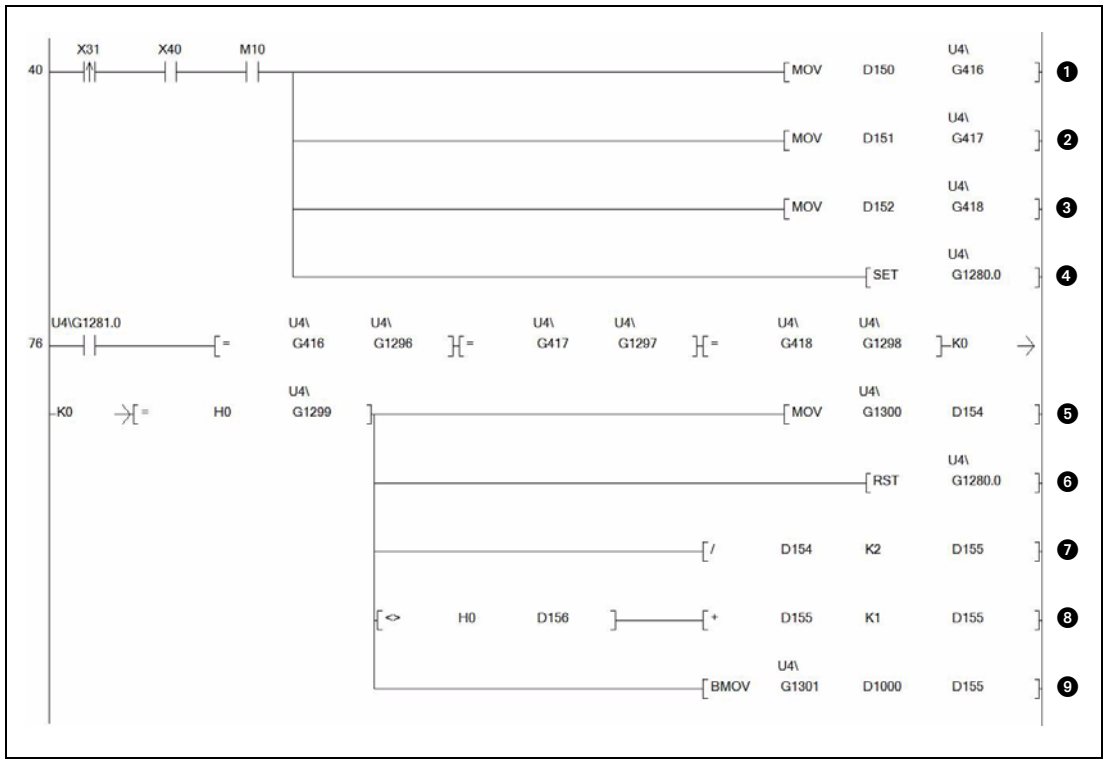


Fig. 6-10: *Program sequence for acyclic communication (reading of data from the IO-Link device)*

Number	Description	
❶	When the module is ready and the initialization of CH1 has been completed without an error, the header information for the communication request is moved to the buffer memory.	Command
❷		Index
❸		Sub-index
❹	The acyclic communication request flag for CH1 is set.	
❺	The number of received bytes is stored in D154. This instruction and the following instructions (❻ to ❾) are only executed when • the acyclic communication response flag for CH1 is set (Un\G1281.0) • the acyclic communication answer area contains the same command, index and subindex as the request • the operation was successful (contents of Un\G1299 = Result = "0000H").	
❻	The acyclic communication request flag for CH1 is reset.	
❼	The data size (unit: bytes) is divided by two in order to get the data size in the unit "words"	
❽	If the result is an odd number (In this case, D156 contains the remainder.), "1" is added to the result. This ensures that all data received will be transferred to the buffer memory.	
❾	The data received from the IO-Link device is stored in registers. The number of points is determined by the contents of D156.	

Tab. 6-10: *Description of the program shown above*

6.5 Example 4: Acyclic Communication (Writing)

System configuration

In this example, data is written to an IO-Link device connected to channel 1 of a ME1IOL6-L using acyclic communication. The same system configuration as for example 1 is used (refer to section 6.2).

Program conditions

- CH1 is used in IO-Link mode (refer to section 4.5.3.).
- The header information for acyclic communication is stored in registers. This allows for an easy change of command, index, subindex, data size and data.

6.5.1 Before creating a program

Before creating the program, perform the steps described in section 6.2.1.

6.5.2 Program

For full documentation of all the instructions used with examples please refer to the Programming Manual for the MELSEC System Q and the MELSEC-L series.

List of used devices

Device		Function		Remark
Inputs	X32	Acyclic communication start signal		LX40C6 (X30 to X3F)
	X40	Module ready		ME1IOL6-L (X40 to X5F)
Internal relay	M10	Initialization of CH1 completed without fault		The mode for CH1 has been changed without fault.
Register	D150	Acyclic communication request	Command	The header information required for the request is stored in these registers by instructions elsewhere in the program.
	D151		Index	
	D152		Sub-index	
	D153		Data size	
	D1200 to D1327	Read to be written to the IO-Link device connected to CH1		The contents of the registers D1200 to D1327 is transferred to the buffer memory addresses Un\G420 to Un\G547. D1200 -> Un\G420 D1201 -> Un\G421 .... D1327 -> Un\G527

Tab. 6-11: *List of used devices for acyclic communication (writing)*

Program parts

- Initial settings

  The initial settings are the same as performed for example 1 (please refer to section 6.2.2).

- Writing of data using acyclic communication

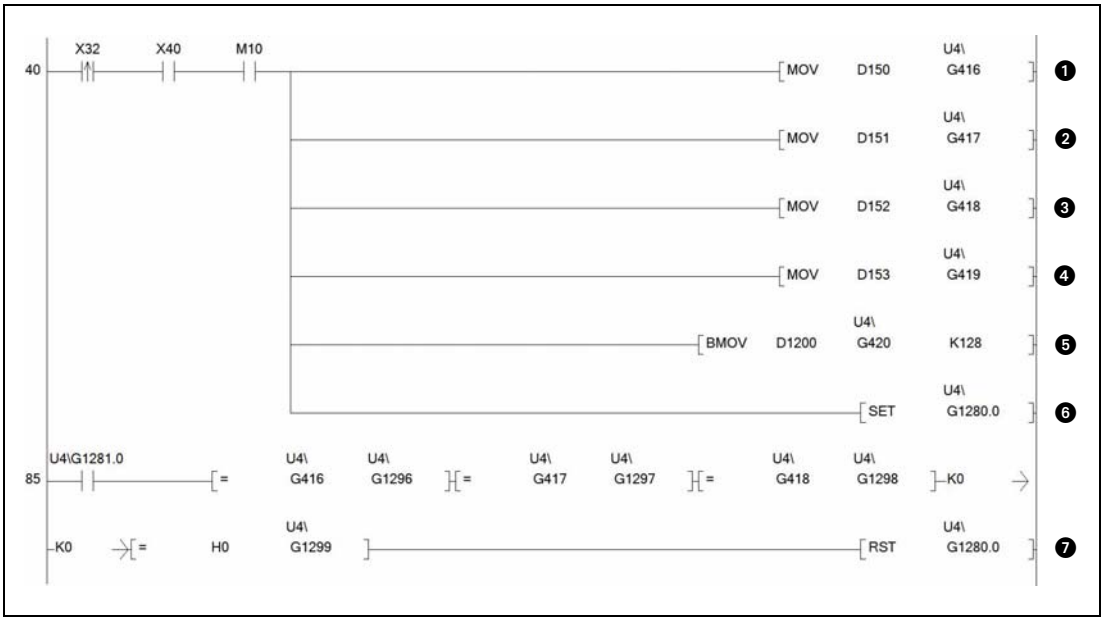


Fig. 6-11: *Program sequence for acyclic communication (reading of data from the IO-Link device)*

Number	Description	
❶	When the module is ready and the initialization of CH1 has been completed without an error, the header information for the communication request is moved to the buffer memory.	Command
❷		Index
❸		Sub-index
❹		Data size
❺	The data intended for the IO-Link device is transferred to the buffer memory.	
❻	The acyclic communication request flag for CH1 is set.	
❼	The acyclic communication request flag for CH1 is reset when • the acyclic communication response flag for CH1 is set (Un\G1281.0) • the acyclic communication answer area contains the same command, index and subindex as the request • the operation was successful (contents of Un\G1299 = Result = "0000H").	

Tab. 6-12: *Description of the program shown above*

7 Troubleshooting

The following section explains the types of errors that may occur when the IO-Link master module ME1IOL6-L is used, and how to troubleshoot such errors.

7.1 Troubleshooting using the LEDs of the Module

This section describes the errors that can be checked with the LEDs on the front of the ME1IOL6-L.

Fig. 7-1:
LED display of the ME1IOL6-L

7.1.1 When the "RUN" LED is turned off

Check item	Corrective action
Is the power being supplied to the PLC?	Confirm that the supply voltage for the power supply module is within the rated range.
Is the capacity of the power supply module adequate?	Calculate the current consumption of the CPU module, I/O modules and intelligent function modules to see if the power supply capacity is adequate.
Has an error occurred in the PLC?	• Confirm the error code and take corrective action (refer to section 7.4.) • Reset the programmable controller CPU and verify that the RUN LED is lit. If it does not light even after doing this, the module may be malfunctioning. Please consult your local Mitsubishi representative, explaining the detailed description of the problem.
Is the module correctly mounted to the CPU module or to an other module?	Check the mounting condition of the module.

Tab. 7-1: *When the "RUN" LED is off*

7.1.2 When any of the LEDs "1" to "6" is off

Check item	Corrective action
Is the corresponding channel deactivated?	Check the current mode of the channel (section 4.5.7).
Is an IO-Link device connected to the corresponding channel when the channel is in IO-Link mode?	Check the connection status of the device (section 5.4.2).
In SIO mode, is the input/output signal OFF?	Check the status of the input/output signals. In SIO mode, the LEDs 1 to 6 indicate the status of these signals. When a LED is OFF, the corresponding signal is OFF too.

Tab. 7-2: *When any off the LED "1" to "6" is off*

7.1.3 When any of the LEDs "1" to "6" lights red

Check item	Corrective action
Has an error occurred on the corresponding channel?	• Check whether the input signal XnF (Error) is ON (refer to section 4.4). • Check the diagnostic information of the channel in the buffer memory (refer to section 4.5.12).

Tab. 7-3: *When any off the LED "1" to "6" lights red*

7.2 Errors related to Process Data

Check item	Corrective action
Is 24 V DC external supply power being supplied?	• Check that the external supply power terminals (terminals 16 (+24V) and17 (24G)) are supplied with a 24 V DC voltage. (In order to keep the specified IO-Link output voltage levels (L+ line) the external supply voltage must be higher than 22 V DC.) • Check that the input signal Xn7 (External power ready) is ON (refer to section 4.4).
Is the ME1IOL6-L working correctly?	• Check that the input signal Xn0 (Module ready) is ON (refer to section 4.4). • Check whether the input signal XnF (Error) is ON (refer to section 4.4). • Check the diagnostic information for the module in the buffer memory (refer to section 4.5.11).
Is the device correctly connected to the ME1IOL6-L?	Check the connection status of the device (section 5.4.2).
Is the connected device working correctly?	Check the device connected to the channel.
Is there any fault with the signal lines such as disconnection or wire break?	Check for faulty condition of the signal lines by a visual check and a continuity check.
Is the CPU module in the STOP status?	Set the CPU module to the RUN status.
Is the mode set for the channel correct?	Verify the contents of the buffer memory addresses 272 to 277 (Un\G272 to Un\G277) in the monitor of GX Works2 (refer to section 4.5.7).
Has an error occurred on the corresponding channel?	• Check whether the input signal XnF (Error) is ON (refer to section 4.4). • Check the diagnostic information of the channel in the buffer memory (refer to section 4.5.12).
What is the status of the data swapping function?	Check whether the data swapping function is activated or deactivated according to the needs of the application (refer to sections 4.3.5 and 4.5.7).
When Input Process Data is wrong	
Is the input data being written to the buffer memory?	• Verify the contents of the buffer memory addresses for the corresponding channel in the monitor of GX Works2 (refer to section 4.5.2). • Check the device connected to the channel.
Is the input data moved from the buffer memory of the ME1IOL6-L to the PLC CPU correctly?	• Check the sequence program. Make sure that the input data is taken out of the correct buffer memory addresses (refer to section 4.5.2). • Check that data is not moved from different sources into the same storage destination in the PLC CPU.
Is consistent data exchanged between an external device and the PLC CPU?	Verify that the correct handshake of signals is executed for the exchange of consistent data. • X(n+1)A to X(n+1)F „Consistent data available“ • Y(n+1)A to Y(n+1)F "Data consistency start signal" (Refer to sections 4.3.6 and 4.4)
When Output Process Data is wrong	
Is the output data being written to the correct buffer memory addresses?	• Verify the contents of the buffer memory addresses for the corresponding channel in the monitor of GX Works2 (refer to section 4.5.3). • Check the sequence program. Make sure that the output data is moved to the correct buffer memory addresses.
Is the signal "Channel □ output data valid" switched ON in order to output the data?	Verify that after writing the output data to the buffer memory, the correspondent output signal (Y(n+1)1to Y(n+1)6) is switched ON (refer to sections 4.3.2, 4.4 and 4.5.3).
Is consistent data exchanged between an external device and the PLC CPU?	Verify that the correct handshake of signals is executed for the exchange of consistent data. • Un\G230 (CH□ Output data consistency enable flag) • Y(n+1)A to Y(n+1)F "Data consistency start signal" (Refer to sections 4.3.6 and 4.4)

Tab. 7-4: *Troubleshooting for process data exchange*

NOTE

If the process data is not read or written after the proper corrective action is taken in accordance with the above check item, the possible cause is a module failure. Please consult your local Mitsubishi representative, explaining the detailed description of the problem.

7.3 Errors related to Acyclic Communication

Check item	Corrective action
Is 24 V DC external supply power being supplied?	• Check that the external supply power terminals (terminals 16 (+24V) and17 (24G)) are supplied with a 24 V DC voltage. (In order to keep the specified IO-Link output voltage levels (L+ line) the external supply voltage must be higher than 22 V DC.) • Check that the input signal Xn7 (External power ready) is ON (refer to section 4.4).
Is the ME1IOL6-L working correctly?	• Check that the input signal Xn0 (Module ready) is ON (refer to section 4.4). • Check whether the input signal XnF (Error) is ON (refer to section 4.4). • Check the diagnostic information for the module in the buffer memory (refer to section 4.5.11).
Is the connected device working correctly?	Check the device connected to the channel.
Is the device correctly connected to the ME1IOL6-L?	Check the connection status of the device (section 5.4.2).
Is there any fault with the signal lines such as disconnection or wire break?	Check for faulty condition of the signal lines by a visual check and a continuity check.
Is the CPU module in the STOP status?	Set the CPU module to the RUN status.
Is the mode set for the channel correct?	Verify the contents of the buffer memory addresses 272 to 277 (Un\G272 to Un\G277) in the monitor of GX Works2 (refer to section 4.5.7).
Has an error occurred on the corresponding channel?	• Check whether the input signal XnF (Error) is ON (refer to section 4.4). • Check the diagnostic information of the channel in the buffer memory (refer to section 4.5.12).
Is the header information for the acyclic communication request correct?	• Verify the contents of the buffer memory addresses for the acyclic communication request in the monitor of GX Works2 (refer to section 4.5.14). • Check the codes for the command, the index and the sub-index. • When writing data, check the data size and the data.
Has the acyclic communication request flag been set?	Make sure that the acyclic communication request flag of the corresponding channel (Un\G1280) is set after the header information has been entered in the buffer memory (refer to sections 4.3.7 and 4.5.15).
Is the acyclic communication response flag set?	Verify that the acyclic communication response flag (Un\G1281) is set by the ME1IOL6-L in response of a communication request (refer to sections 4.3.7 and 4.5.16).
Is the header information sent in the answer correct?	The codes for the command, the index and the sub-index sent in the answer should read the same as in the acyclic communication request (refer to section 4.5.17).
Is the result code equal to 0000_H?	Check the result code for the communication request. If the result code is not equal to 0000_H, an error has occurred while performing acyclic communication (section 4.5.17).
Is the data swapping function set correctly?	Check whether the data swapping function is activated or deactivated according to the needs of the application (refer to sections 4.3.5 and 4.5.7).

Tab. 7-5: *Troubleshooting for acyclic communication*

7.4 Checking the IO-Link Master Module Status

When the IO-Link master module detailed information is selected in the system monitor of GX Works2 (**Diagnostics** menu -> ***System Monitor***), the status of the module can be checked.

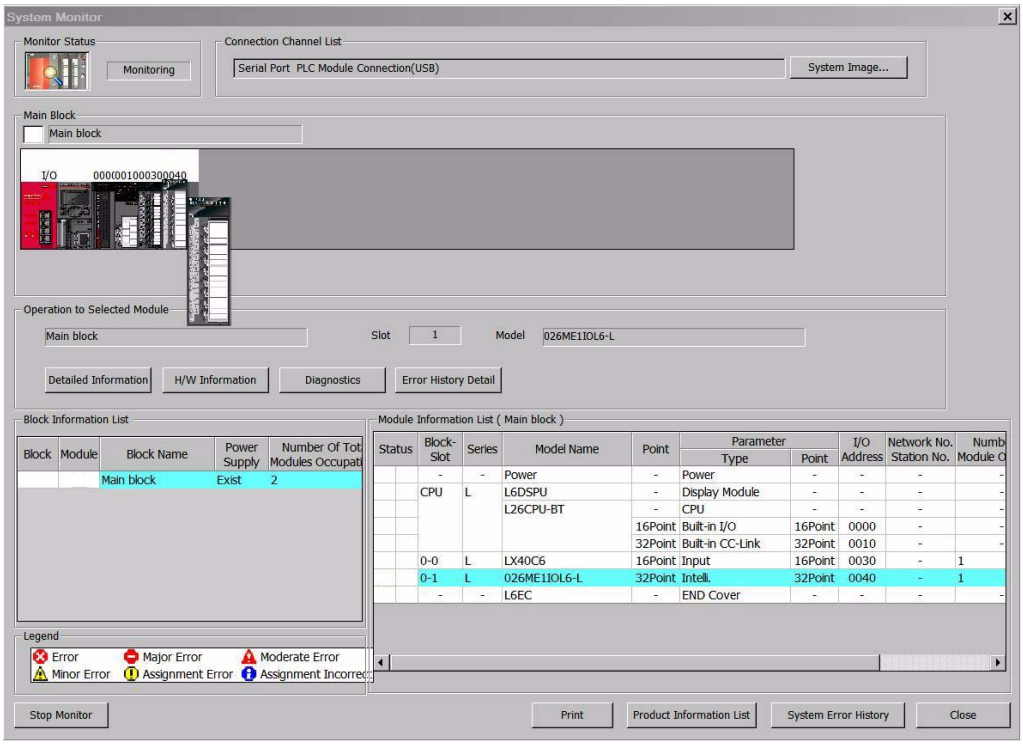


Fig. 7-2: *The System Monitor displays comprehensive information of the connected PLC*

For further information about a module, click on the module and then click ***Detailed Information*** (see next page).

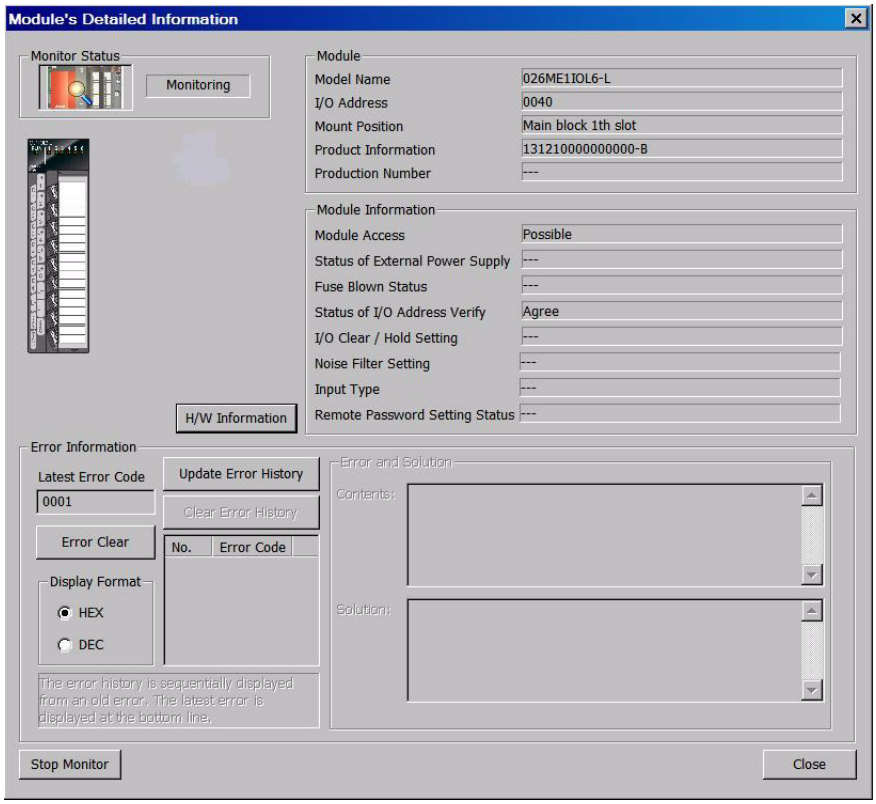


Fig. 7-3: *Detailed information on the selected module allow an easy and quick troubleshooting*

Contents of Module's Detailed Information

- Module
  - Module Name: Shows the designation of the module, e.g. ME1IOL6-L
  - I/O Address: Head address of the module
  - Mount Position: Shows where in the PLC the module is mounted.
  - Product information: Serial No. of the module. The letter shows the function version.
  - Production Number
- Module Information
  - Module Access: Shows whether the module is ready or not.
  - Status of external power supply: Not relevant for the ME1IOL6-L.
  - Fuse blown status: Not relevant for the ME1IOL6-L.
  - Status of I/O Address Verify: Indicates whether the parameter set module and the installed module are identical.
  - I/O Clear / Hold Settings: Not relevant for the ME1IOL6-L.
  - Noise Filter Setting, etc.: Not relevant for the ME1IOL6-L.
- Error Display

  No error codes are issued by the ME1IOL6-L.

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